Serial communication

Serial to Parallel

Parallel output

Output latch

Address matching

Serial input

clock

clear

Data bits (4 LSB)

If address matches, latch the data

Address bits (4 MSB)

addr data

Sample sequence: 10111010
Serial communication

Serial input: 1011010

Clock:

Serial to Parallel

Parallel output:

Clear output:

BUS:

Address matching:

Data bits (4 LSB):

Match:

If address matches, latch the data:

Addr data:

Sample sequence: 1011010
Serial communication

Serial communication

Serial to Parallel

BUS

Address matching

Output latch 1101
Input sequence: 10111010

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared

Device address

address to compare: 1011
Input sequence: 10111010

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared

address to compare: 1011
Serial communication

Input sequence: 1011 1010

Address to compare: 1011

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared.

Device address: 1011

Address to compare: 1011

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared.
Serial communication

Device address: 1011

Input sequence: 10111010

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared

address to compare: 1011
Serial communication

Input sequence: 1011 1010

Device address 1011

P0...P3 and Q0...Q3 set to ’1’, so only bits 4...7 are compared

address to compare: 1011
Serial communication

Input sequence: 1011 1010

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared

Device address 1011

address to compare: 1011
Serial communication

Input sequence: 10111010

P0...P3 and Q0...Q3 set to '1', so only bits 4...7 are compared.

address to compare: 1011

Device address: 1011

10111010
Serial communication

Input sequence: 10111010

1011

Device address

P0...P3 and Q0...Q3 set to ’1’, so only bits 4...7 are compared

address to compare: 1011
Serial communication

Input sequence: 1011 1010

Comparison: 1011 1111 and 1011 1111

match

address to compare: 1011
Input sequence: 10111010

Comparison: 10111111 and 10111111

match

address to compare: 1011

Device address

Comparison: 10111111 and 10111111
match

address to compare: 1011

Input sequence: 10111010
Serial communication

Input sequence: 10111010

Comparison: 1011 1111 and 1011 1111 match

address to compare: 1011
Experiments

1. Implement 4-bit serial transmission with one receiver
2. Implement 4-bit serial transmission with multiple receivers
3. Implement 4-bit serial transmission with one receiver and parity check