**CPE 200L**
**LOGIC DESIGN II**

**LABORATORY 3:**
**CLOCK GENERATION AND ALU**
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**GOALS:**
Understand the concept of inverter voltage transfer characteristics, clock, gate delays and simple combinatorial circuit design. In this lab we will cascade an odd number of inverters to create a ring oscillator and build a 4 bit ripple carry adder. Three bitwise functions will be added to FA to constitute 2-bit ALU.

**BACKGROUND:**

**INVERTER VOLTAGE TRANSFER CHARACTERISTICS**
An inverter’s voltage transfer characteristic is shown below is obtained by continuously varying the input voltage on the x-axis. Y-axis depicts the voltage measured at the output.

![Inverter Voltage Characteristics](image)

*Figure 1. Inverter Voltage Characteristics*

For the input of an inverter, the voltage range from Ground (0 Volts) to $V_{IL}$ represent
logic ‘0’ and $V_{IH}$ to $V_{DD}$ represent logic ‘1’. Logic level between these regions is undefined and occurs only during logic transition in digital systems.

Noise margins $N_{MH}$ and $N_{ML}$ define maximum input excursions that can be tolerated without introducing logic errors. High level of noise margin allows greater cushion for noise immunity.

**RING OSCILLATOR**

An odd number of inverters connected in a ring form an oscillator, whose frequency of oscillation is a function of number of stages and delay of the inverter used. A five stage ring oscillator is shown below:

![Five-Stage Ring Oscillator](image)

To understand the operation of ring oscillator above, assume that input value at ‘A’ is ‘1’. If the delay of each inverter is $\tau$, after $n\tau$ ($n=5$ in the figure above) period, ‘0’ is fed back at the same input. Therefore, cycle time of the oscillator is $2n\tau$ and frequency of oscillation is $f = \frac{1}{T} = \frac{1}{2\pi\tau}$

**LOGIC MINIMIZATION**

Logic minimization techniques reduce the number of logic gates required to implement a Boolean function. The three most popular logic minimization techniques are Quine-McCluskey Algorithm, Espresso heuristic and Karnaugh-Maps.

1. **Quine-McClusky Method**: This is an ‘exact’ method, which generates a solution with the fewest product terms. However, this method requires a lot of computation.
2. **Espresso Heuristic Methods**: These methods can achieve results that are as good as the Q-M approach with less computational overhead.
3. **Karnaugh Maps**: This is a visual method of Q-M algorithm and works only on function up to 6 variables at the most.
**LAB DELIVERIES:**

**PRELAB:**

1. **Full Adder Design:**
   1. Construct a truth table of full adder circuit including the sum and carry out outputs.
   2. Write the equation for each output that minimizes number of gates required for implementation.
   3. Create a gate level schematic of your design using the schematic editor such as Altera Quartus. Perform gate level simulation of the circuit. Refer to the class website for tutorial on using Altera Quartus.

![Figure 3. Full Adder](image)

2. **ALU Design:**
   1. Construct 2-bit ALU, including your FA.
   2. It will have the following inputs and outputs:
      - \( a_0 \) – first (less significant) bit of first argument
      - \( a_1 \) – second (most significant) bit of first argument
      - \( b_0 \) – first (less significant) bit of second argument
      - \( b_1 \) – second (most significant) bit of second argument
      - \( c_0 \) – first (less significant) bit of operation selection
      - \( c_1 \) – second (most significant) bit of operation selection
      - \( y_0 \) – first (less significant) bit of the output result
      - \( y_1 \) – second (most significant) bit of the output result
      - \( cout \) – carry out from full adder

![Figure 4. ALU](image)
3. Functions that ALU is equipped with:
   a. Arithmetic ADD
   b. Bitwise XOR
   c. Bitwise AND
   d. Bitwise OR
4. Use 4-to-1 multiplexer to switch between functions.

3. **Prelab deliveries**
   Include in the report document:
   1. Full adder function derived
   2. Full adder minimization
   3. Full adder schematic created in Quartus
   4. Full adder simulation waveform generated by Quartus
   5. ALU schematic created in Quartus
   6. ALU simulation waveform generated by Quartus

**LAB EXPERIMENTS:**

1. **Experiment 1: Ring oscillator**
   1. Construct a clock generation circuit using five stage ring oscillator.
      a. Demonstrate the output of the oscillator on oscilloscope by connecting the output of any inverter to one of the oscilloscope channel (press “auto trigger” to the channel connected).
      b. Calculate delay of the channel and period of the oscillation.
   2. Demonstrate the operation to the TA.

2. **Experiment 2: Full Adder**
   1. Implement your full adder circuit and demonstrate your circuit output to TA by connecting outputs to LED (use a 1k resistor in series with LED to limit current through LED).

3. **Experiment 3: Ripple Carry Adder**
   1. Implement a two bit ripple carry adder as shown on the schematic from Figure 5.
   2. Demonstrate your circuit output to TA by connecting outputs to LED (use a 1k resistor in series with LED to limit current through LED).

4. **Experiment 4: ALU**
   1. Implement your ALU design on the board
   2. Demonstrate the operation to TA.
Figure 5. Ripple Carry Adder
**POSTLAB REPORT:**

Include the following elements in the report document:

<table>
<thead>
<tr>
<th>Section</th>
<th>Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Theory of operation</td>
</tr>
<tr>
<td></td>
<td>Include a brief description of every element and phenomenon that appears during the experiments.</td>
</tr>
<tr>
<td>2</td>
<td>Prelab report</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Experiment</th>
<th>Element Results</th>
</tr>
</thead>
</table>
| 1          | a. Screenshot of the oscilloscope screen, showing the oscillation  
|            | b. Derived inverter delay from the period of oscillation (show how it was derived)  
|            | c. Picture of the breadboard with the schematic     |
| 2          | a. Truth table                                       |
|            | b. Screenshot of the schematic from Quartus          |
|            | c. Picture of the breadboard with the schematic      |
| 3          | a. Truth table                                       |
|            | b. Screenshot of the schematic from Quartus          |
|            | a. Picture of the breadboard with the schematic      |
| 4          | a. Truth table                                       |
|            | b. Description of what control values are activating which ALU signal  
|            | c. Screenshot of the schematic from Quartus          |
|            | a. Picture of the breadboard with the schematic      |

Answer the questions

<table>
<thead>
<tr>
<th>Question no.</th>
<th>Question</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>If the gate delay is 5ns, what would be the frequency of oscillation for 21 stage ring oscillator?</td>
</tr>
<tr>
<td>2</td>
<td>Are the signals at P, Q, R and S in Figure 2 periodic? If so, what is their period? How do they differ from the signal at A?</td>
</tr>
<tr>
<td>3</td>
<td>Draw schematic of your two bit ripple carry adder. Assuming each gate has identical delay, find the maximum delay path (which is also known as critical path).</td>
</tr>
</tbody>
</table>

Conclusions

Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.

Attachments

Zip your projects. Send through email as attachments, or provide link to the zip file on Google Drive / Dropbox, etc.

List of attachments to deliver:

1. Full Adder Quartus project
2. ALU Quartus project

References:
