CPE 200L Logic Design II

LABORATORY 3:
SEQUENTIAL LOGIC CIRCUITS

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
UNIVERSITY OF NEVADA, LAS VEGAS

GOALS:

Learn to use Function Generator and Oscilloscope on the breadboard. Use a flip flop correctly. Use a square wave from Function Generator as CLK to FF. Learn how to use 7-segment display. Learn the usage of flipflops.

BACKGROUND:

Flip-flops are the simple sequential elements, which state depends not only on input signals, but also on previous flipflop states. Following are brief paragraphs about flip-flops.

SR FLIP-FLOP/LATCH

This is basic Set/Reset flipflop. Two inputs are used to to set or reset outputs. Both of these actions are not available at the same time (you cannot set and reset at the same time) so this combination of inputs is not allowed.

![SR Flip-flop diagram]

Table 1. SR Flip-Flop operation

<table>
<thead>
<tr>
<th>State</th>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Set Q → 1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Unchanged</td>
</tr>
<tr>
<td>Reset</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Reset Q → 0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Unchanged</td>
</tr>
<tr>
<td>Invalid</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Invalid state</td>
</tr>
</tbody>
</table>
**JK Flip-Flop**

This is the extended version of Set/Reset flipflop. It allows all combinations of inputs. Providing J=1 and K=1 toggles the flipflop state.

![Figure 2. JK Flip-flop](image)

<table>
<thead>
<tr>
<th>State</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Same as SR</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No change</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Reset Q → 0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Set Q → 1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>toggle</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Toggle</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**D Flip-Flop**

D flip-flop passes the signal from D input to the output, when clock is in active edge state.

![Figure 3. D Flip-flop](image)

<table>
<thead>
<tr>
<th>CLK</th>
<th>D</th>
<th>Q</th>
<th>Q</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>↓ (0)</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
<td>No change</td>
</tr>
<tr>
<td>↑ (1)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reset Q → 0</td>
</tr>
<tr>
<td>↑ (1)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Set Q → 1</td>
</tr>
</tbody>
</table>
T Flip-Flop

When T=1, then active clock strobe toggles the output state of the flipflop.

![T Flip-flop diagram](image)

Figure 4. T Flip-flop

Example of flipflop use: organization of 1-bit memory

![1-bit memory cell diagram](image)

Figure 5. 1-bit memory cell

Debouncing Circuit

SR Latch:
The S-R latch has two inputs and two outputs. One output is the complement of the other. The S input “sets” the output (to logic „1“) while the R “resets” the output to logic „0“. Figure 6 below shows the schematic and truth table for the S-R latch.

![SR Latch diagram](image)

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q(n)</th>
<th>Q(n+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q(n)</td>
<td>Q(n)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>NA</td>
</tr>
</tbody>
</table>

Figure 6. SR Latch
**Push Button:**
It is a mechanical device and relies on mechanical contact to generate electrical signal. Once a push button is pressed, signal generated by the push button is as follows:

![Figure 7. Push button generated signal](image)

As seen from above, such signal is quite choppy and needs to be cleaned using de-bouncing circuit before it can be applied to digital circuit. Many de-bouncing circuit design exist such as Latch based, Sampling based, Software based, etc. A SR latch based de-bouncing circuit is shown below:

![Figure 8: SR Latch based de-bouncer](image)

Assume that the switch is normally connected to the S (set) input of the SR latch as illustrated in Figure 8. Therefore, the S input is pulled to a logical 0 and the Q output to a logical 1, which is the Set state of the SR latch. When the switch is pushed, the latch inputs transition from S=0 and R=1 to S=1 and R=1, corresponding to the storage state where the Q output continues to be a logical 1. Glitches at the S input take the latch from the set state to the storage state, keeping the Q output at a logical 1. Once the switch contacts the R input, the inputs to the latch change from S=1 and R=1 to S=1 and R=0, corresponding to the reset state which produces a logical 0 at the Q output. Subsequent glitches at the input keep the latch between reset state and the storage state keeping Q unchanged. Note that the double-pole switch at the inputs of the SR latch prevents the latch from entering the indeterminate state where both S and R are 0 and both the Q and Q bar outputs are forced to a logical 1.
COUNTER

Counter is a sequential circuit, where output is a function of both current and past inputs. It counts up/down at clocked signal either at rising edge or falling edge. Counter uses memory elements such as SR latch to keep track of current state and increment or decrement it at every clock pulse.

Example:
Let’s design a 2-bit synchronous counter with transition states as shown in Figure 10.

To design the counter, we must first construct transition table. The transition table shows the state output values after the clock pulse (next) as a function of the input and state output values before the clock pulse (now). Since for a D type flip-flop the output (Q) after the clock pulse is equal to the input (D) before the clock pulse, the transition table becomes a simple input/output truth table. Transition table and K-map minimization of the counter are shown below:
After simplification, we derive the following:

\[ D1 = Q1' \cdot Q2 + Q1 \cdot Q2' = Q1 \oplus Q2 \]
\[ D2 = Q2' \]

Final schematic of the 2-bit counter is as follows:

Figure 12. 2-bit Synchronous Counter Circuit

7-SEGMENT DISPLAY

Binary coded decimal (BCD) numbers are often displayed on seven segment display using BCD to seven segment decoder such as 7447, which we use in this lab. Figure 13 illustrates BCD to seven segment display circuit.
There are two configurations of 7-segment displays: common anode and common cathode. In this lab we use common anode type, what can be illustrated as follows:

Figure 14. Common anode configuration

Figure 15 shows complete schematics for 7-segment and 7447 driver configuration. 7447 takes BCD number as the input and converts to 7-signal format, as shown in truth table further. Do not forget about the 2.4 kΩ resistor, to limit the current.

Figure 15. Schematics for 7-seg with 7447 configuration
**LAB DELIVERIES:**

**PRELAB:**

1. **Counter**
   1. Read the tutorial on how to use a breadboard.
   2. Simulate 3 bit synchronous counter and verify truth table.

2. **Prelab deliveries**
   Include in the prelab document:
   1. Your design of 3-bit counter
   2. Simulation waveforms of 3-bit counter

**LAB EXPERIMENTS**

To find the chip implementing the desired function, or to look for the datasheet regarding the specific chip, go to [https://faculty.unlv.edu/eelabs/index.html?navi=main_icdatasheets](https://faculty.unlv.edu/eelabs/index.html?navi=main_icdatasheets)

1. **Experiment 1: Function Generator and Oscilloscope on Breadboard with Chips**
   Use the Function Generator to set up a square wave 0V-5V, frequency 1kHz. Apply to the input of an inverter/NOT gate. Use Channel 1 of oscilloscope to see input, and channel 2 to see the output. Verify the operation of the NOT gate.

![Schematic for experiment 1](function_generator_oscilloscope.png)

   **Figure 16. Schematic for experiment 1**

2. **Experiment 2: Use of JK Flip Flop**
   Use the square wave of 0V-5V, frequency 1kHz from Function Generator as the CLK input to JKFF.

   a) Implement T flip flop. There are no T flip flop chips. Use the JK flip flop (JK is universal) as a T flip flop (do the conversion J=K=T). Let T=1 to have it toggle. Use Channel 1 of oscilloscope to see CLK input, and channel 2 to see the Q output. Verify that the output Q is a frequency divider (divide by 2).
b) Use JKFF as a DFF (J=K’=D). Let D=Q. Use Channel 1 of oscilloscope to see CLK input, and channel 2 to see the Q output. Verify that the output Q is a frequency divider (divide by 2).

![Oscilloscope CH2](T configuration)

![Oscilloscope CH2](D configuration)

Figure 17. Setups for experiment 2

3. **Experiment 3: Use a 7-Segment Display with 7447 Decoder**
   1. Connect a 7447 Decoder with 7-Segment Display. Ensure that the binary number input for the 7447 decoder shows up correctly in the 7-segment display for numbers 0-9.

   ![7447 decoder](a0 a1 a2)

   Figure 18. BCD to 7-segment conversion

   Inputs a0, a1, a2 are three separate wires. Connect them to 5V or GND to set the BCD combination.

4. **Experiment 4: 3-bit counter**
   1. Implement a 3 bit synchronous counter using flipflops from Experiment 3 (already verified). Use the CLK from the function generator at a frequency of 1 Hz (for humans to see). Connect the output of the counter to the 7-segment circuit using configuration from experiment 3. Verify it counts from 0 to 7.
Figure 19. 3-bit counter with function generator and 7-segment display

2. Replace the function generator input with the mechanical switch. Is the bouncing effect occurring?

Figure 20. 3-bit counter with mechanical switch and 7-segment display

Apply the debouncing circuit:

Figure 21. 3-bit counter with mechanical switch, debouncer and 7-segment display
POSTLAB REPORT:

Include the following elements in the report document:

<table>
<thead>
<tr>
<th>Section</th>
<th>Element</th>
</tr>
</thead>
</table>
| 1       | Theory of operation  
Include a brief description of every element and phenomenon that appears during the experiments. |
| 2       | Prelab report |
| 3       | Results of the experiments |
| Experiment | Element |
| 4       | a. Drawing of schematic  
b. Picture of the circuit on the breadboard  
c. Picture of the waveforms from the oscilloscope |
| 5       | a. Drawing of schematic  
b. Picture of the circuit on the breadboard  
c. Picture(s) of the operation |
| 6       | a. Drawing of schematic  
b. Picture of the circuit on the breadboard  
c. Picture(s) of the operation |

<table>
<thead>
<tr>
<th>Question no.</th>
<th>Question</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Find various 74xx chips for JKFF. What are differences?</td>
</tr>
<tr>
<td>2</td>
<td>List types of BCD-to-7seg decoders along with short description</td>
</tr>
<tr>
<td>3</td>
<td>What is debouncing problem?</td>
</tr>
</tbody>
</table>

Conclusions  
Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.

References:
1. Introduction to breadboards: [http://faculty.unlv.edu/eelabs/docs/equipment/breadboards.pdf](http://faculty.unlv.edu/eelabs/docs/equipment/breadboards.pdf)