University of Nevada, Las Vegas
Department of Electrical and Computer Engineering

CPE 200L Computer

Logic Design II
Laboratory

Prepared and Revised by
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August 2013
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Overview

Introduction
This lab course will introduce you to the principles of digital system design with low complexity so that final design can be implemented with basic digital gates. We will utilize hardware description language to facilitate smooth design flow.

Requirements
This class is comprised of ten laboratory exercises (some of which may take multiple weeks). Each lab will have a laboratory write-up, and most of the laboratories will have a prelab. The purpose of the prelab is to insure that the student has examined the lab and has prepared for it. Preparation is vital to safe, accurate, and productive work. Make sure to ALWAYS read the lab in full before coming to class.

Guidelines for the lab report are posted on the class website. You must follow the guidelines if you wish to get the credit for the lab report.

All lab reports must be submitted within a week after the experiment both in hardcopy and electronically. No exceptions.

Carefully read lab experiment handouts prior to start of the lab. Any ambiguity encountered must be brought to the attention of the instructor immediately. Be sure to complete pre-lab prior to coming to the class. Grading will be weighted as follows:

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<td>Prelab</td>
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<td>Postlabs</td>
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<td>Lab activity</td>
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Help
In class the TA is there to help. He/she will be available to answer all questions and should be utilized often. In addition to the TA, lab instructor is always available to answer any questions. Finally, fellow students are also a good source of information and help. However, all work must be performed individually and all reports are to be turned in individually.

On rare occasions, it may be necessary to miss a lab class. With a valid excuse, a make-up session can be arranged.

To help facilitate your learning process, please provide written feedback in a timely manner to help us modify lab experiments as necessary.
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Labs Overview
Laboratory Exercise 1 – Lab safety and Equipment Use
Laboratory Exercise 2 – Digital Logic Characteristics, De-bouncing Circuit, Counter
Laboratory Exercise 3 – Clock generation & ALU
Laboratory Exercise 4 – Introduction to DE2 board
Laboratory Exercise 5 – Serial Communication
Laboratory Exercise 6 – Random Number Generation
Laboratory Exercise 7 – Multiplier Design
Laboratory Exercise 8 – Altera Nios II Processor
Laboratory Exercise 9 – Altera Nios II Logic Instructions
Laboratory Exercise 10 – A Simple Processor
Laboratory Exercise 11 – An Enhanced Processor
Laboratory Exercise 10 – Final Project