LABORATORY 4:  
INTRODUCTION TO DE0 BOARD  
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GOALS:

Getting familiar with DE0 board installation, properties, usage. Programming simple circuit using Altera Quartus.

BACKGROUND:

Altera’s DE0 Development and Education Board has been developed to provide an ideal vehicle for learning about digital logic and computer organization in a laboratory setting. It uses the state-of-the-art technology in both hardware and CAD tools to expose students to a wide range of topics covered in typical courses. The power of the board is such that it is also highly suitable for a variety of design projects as well as for the development of sophisticated digital systems. In addition to the DE0 board and the associated software, Altera provides supporting materials that include tutorials, laboratory exercises, and interesting demonstrations [1].

The DE0 Development and Education board is designed in a compact size with all the essential tools for novice users to gain knowledge in areas of digital logic, computer organization and FPGAs. It is equipped with Altera Cyclone III 3C16 FPGA device, which offers 15,408 LEs. The board provides 346 user I/O pins, and is loaded with a rich set of features that makes it suitable to be used for advanced university and college courses, as well as the development of sophisticated digital systems. The DE0 combines the Altera low-power, low-cost, and high performance Cyclone III FPGA to control the various features of the DE0 Board. The DE0 Development Board includes software, reference designs, and accessories required to ensure the user simple access in evaluating their DE0 Board. Continue reading at http://faculty.unlv.edu/eelabs/docs/guides/DE0_CV_User_Manual.pdf
SETTING UP DE0-CV BOARD:

The following procedure configures DE0-CV on the PC computer. Please note, that for TBE-B350 and TBE-B311 labs, the effects of this procedure will disappear when you log out of lab station computer. You have to repeat the procedure at the start of each lab if you plan to work with DE0-CV board.

1. Plug the DC adapter
2. Connect board using USB to the PC computer. Remember to use leftmost connector
3. Click ‘Start’, right-click ‘Computer’ and select ‘Properties’:

![Image of USB connection and Windows properties]

Download DE0-CV C:
http://cd-de0-cv.ten
Click ‘Device manager’:

You will see the list of devices, look for ‘USB-Blaster’, should be under the section ‘Other devices’:
Click ‘Update driver’:

Use ‘Browse my computer for driver software’:
Browse to: “C:\altera\13.1\quartus\drivers”

After clicking ‘Next’, the following popup can appear:

Answer “Install this driver software anyway”: 
If the installation is successful, you should receive:

![Driver Software Update]

Windows has successfully updated your driver software.

![Driver Properties]

This device is working properly.
IMPLEMENTING SIMPLE PROJECT IN QUARTUS

The workflow of executing the project on DE0-CV board is as follows:

First three steps are described in *Simulating Design in Quartus 13.1* document. Please refer to this document to see how to get the compiled project.

PROGRAMMING DE0 BOARD

To proceed with the following steps, you have to have:
1. DE0-CV board configured in Windows system (section 1 of this instruction)
2. Schematic design compiled (*Simulating Design in Quartus 13.1* document [1])

Once you have these two steps ready, the following steps are done in Quartus with your project opened.

1. Specify the device
   In this case DE0-CV with chip: *Family Cyclone V, Device 5CEBA4F23C7.*

   Go to Assignments -> Device
Device selection screen appears:

Select Family Cyclone V and then use the Name Filter to locate the 5CEBA4F23C7 device. Select the device from the Available devices list and click OK.

2. **Assign pins**
   Go to Assignments -> Pin Planner.
New window of *Pin Planner* will pop up:

The *Location* determines, where your *schematic pin* will be connected to *hardware onboard pin*.

Inputs can be connected* to switches (SW0-SW9) and pushbuttons (KEY0-KEY3):

Outputs can be connected* to LEDs (Light Emitting Diodes) (LEDR-0-LEDR9):

*among others
When input $a$ is connected to switch SW0, then this switch can be used to set the value of $a$. When output $y$ is connected to LEDR0, then the value of $y$ can be observed on this LED.

To determine the hardware location of switches, pushbuttons, LEDs etc. – please refer to DE0 Pin Table [2] or Altera DE0 Introduction / User Manual [3]. Based on the tables on page 24 and 25 of User Manual:

- Switch SW0 is located at pin PIN_U13
- Switch SW1 is located at pin PIN_V13
- LED LEDR0 is located at pin PIN-AA2

Therefore, the following assignments are done:

<table>
<thead>
<tr>
<th>Node Name</th>
<th>Direction</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>in_a</td>
<td>Input</td>
<td>PIN_U13</td>
</tr>
<tr>
<td>in_b</td>
<td>Input</td>
<td>PIN_V13</td>
</tr>
<tr>
<td>out_y</td>
<td>Output</td>
<td>PIN-AA2</td>
</tr>
</tbody>
</table>

So switch SW0 will control the value of $a$, switch SW1 will control the value of $b$, and the result value of $y$ will be displayed on LEDR0.

Close Pin Planner. You can see that assignments are now visible on the schematic.

Compile the project.

3. Upload the design to the board

Make sure, that RUN/PROG switch is in the RUN position.

Select Tools -> Programmer.
The *Programmer* tool pops up:

No hardware is configured yet. Click *Hardware Setup* and select *USB-Blaster* from the *Currently Selected Hardware* dropdown and click *Close.*
Click *Hardware Setup* and select *USB-Blaster* from drop-down list.

Ensure that *Mode* value is set to *JTAG*.

Click *Add File* option and choose *lab4.sof* (or other *.sof* file that is the result of your compilation). Look for this file in your project directory's subdirectory *output_files*. Make sure that *Program/Configure* checkbox is checked.

Click *Start* and wait for the board to be programmed. Observe System Messages to see if programming process ended with success.

Progress: **100% (Successful)**
The board is now programmed. Two switches serve as $a$, $b$ inputs to the gate, while the logic state of the output $y$ is signaled by red LED.

For more information, refer to Altera’s *DE0 Board User Manual* [3]: [http://faculty.unlv.edu/eelabs/docs/guides/DE0.CV_User_Manual.pdf](http://faculty.unlv.edu/eelabs/docs/guides/DE0.CV_User_Manual.pdf) and *Altera DE0 Computer System* [4]: [http://faculty.unlv.edu/eelabs/docs/guides/DE0.CV_Computer.pdf](http://faculty.unlv.edu/eelabs/docs/guides/DE0.CV_Computer.pdf)
**TROUBLESHOOTING**

Quartus schematics:
- Compilation errors:
  - Make sure schematic does not contain any floating elements
  - Make sure that all input and output pins are connected to the elements
- No pins showing in node finder:
  - Make sure you have performed Compilation
  - Make sure you have performed Analysis & Synthesis
- Output signal changes with delay to input signals:
  - This is probably correct – for Timing simulation. Probably you expect Functional simulation. Set that in Simulation Options.

Programming the board:
- Quartus does not see the board:
  - Make sure that USB-Blaster is installed
  - Make sure that Windows device manager indicates that USB-Blaster device works properly
  - Make sure you connected USB cable to BLASTER port on the board
- Board is visible, but there are errors while programming the board:
  - Make sure that Family and Device values are set exactly to ones that you can read from FPGA chip on your board
  - Make sure that RUN/PROG switch is in RUN position

**LAB DELIVERIES:**

**PRELAB:**

1. **Get familiar with Altera DE0 introduction documents**
   Make yourself familiar with the following documents:
   - *DE0-CV Board User Manual*:
   - *Altera DE0-CV Computer*:
     [http://faculty.unlv.edu/eelabs/docs/guides/DE0_CV_Computer.pdf](http://faculty.unlv.edu/eelabs/docs/guides/DE0_CV_Computer.pdf)

2. **Prelab deliveries**
   Write few paragraphs about FPGA technology
LAB EXPERIMENTS:

1. **Experiment 1: Configure DE0 board in Windows system**
   Use either the chapter ‘Setting Up DE0-CV Board’ from this lab instruction to setup the DE0-CV board. Follow the document *Simulating Design in Quartus 13.1* [1] and implement the XOR gate on the DE0-CV board. Demonstrate working XOR to the TA.

2. **Implementing functions**
   a) Create new project, and implement functions a) – d).
   
   a) \( F_1 = AB + A'B' \)
   b) \( F_2 = CD + C'D \)
   c) \( F_3 = (E+G)(E'+G') \)
   d) \( F_4 = HIJ + H'I'J + H'JI \)

   For inputs A-J use separate switches. For outputs \( F_1-F_4 \) use separate LEDs. This means, that these four functions need to work concurrently on the DE0 board within one project, and they work independently of each other.

POSTLAB REPORT:

Include the following elements in the report document:

<table>
<thead>
<tr>
<th>Section</th>
<th>Element</th>
</tr>
</thead>
</table>
| 1       | Theory of operation  
Include a brief description of every element and phenomenon that appears during the experiments. |
| 2       | Prelab report |
| 3       | Results of the experiments  
| Experiment | Experiment Results |
| 1       | a. Quartus Schematic  
b. Simulation Output  
c. Summary of your experience with DE0 board, including problems you experienced and how they were solved. |
| 2       | a. Quartus Schematic  
b. Simulation Output |
| 4       | Answer the questions  
| Question no. | Question |
| 1       | What is a sof file? |
| 2       | What is the difference between RUN and PROG modes of DE0 board? |
| 3       | What is the Cyclone V chip and where it is used? |
| 5       | Conclusions  
Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc. |
| 6       | Attachments  
Zip your projects. Send through WebCampus as attachments, or provide link to the zip file on Google Drive / Dropbox, etc.  
List of attachments to deliver:  
1. Quartus project you did in class (project with four functions in it). |
References:
1. *Simulating Design in Quartus 13.1*
   http://faculty.unlv.edu/eelabs/docs/guides/Simulating_Design_in_Quartus_13_1.pdf
2. DE0 pin table: http://faculty.unlv.edu/eelabs/docs/guides/DE0_Pin_Table.pdf
3. *Altera DE0 Introduction / User Manual*
4. *Altera DE0 Computer System*
   http://faculty.unlv.edu/eelabs/docs/guides/DE0.CV_Computer.pdf
5. Datasheets of 7400 series chips:
   http://faculty.unlv.edu/eelabs/index.html?navi=main_icdatasheets