CPE 100L  LOGIC DESIGN I

LABORATORY 2:
INTRODUCTION TO DIGITAL LOGIC GATES AND SIMPLE BOOLEAN IMPLEMENTATION

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GOALS:
Understand function of digital logic gates and implement simple combination circuit and gain experience of design flow.

BACKGROUND:
Boolean algebra is the oldest method used to minimize logic equations. It provides a formal algebraic system that can be used to manipulate logic equations in an attempt to find more minimal equations. It is a proper algebraic system, with three set elements {‘0’, ‘1’, and ‘A’} (where ‘A’ is any variable that can assume the values ‘0’ or ‘1’), two binary operations (and or intersection, or or union), and one unary operation (inversion or complementation). Operations between sets are closed under the three operations. The basic laws governing and, or, and inversion operations are easily derived from the logic truth tables for those operations.

Truth tables of basic gate operations is as follows:

<table>
<thead>
<tr>
<th>AND operations</th>
<th>OR operations</th>
<th>INV operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Truth table</td>
<td>Laws</td>
<td>Truth table</td>
</tr>
<tr>
<td>0 · 0 = 0</td>
<td>A · 0 = 0</td>
<td>0 + 0 = 0</td>
</tr>
<tr>
<td>1 · 0 = 0</td>
<td>A · 1 = A</td>
<td>1 + 0 = 1</td>
</tr>
<tr>
<td>0 · 1 = 0</td>
<td>A · A' = 0</td>
<td>0 + 1 = 1</td>
</tr>
<tr>
<td>1 · 1 = 1</td>
<td>A · A' = 0</td>
<td>1 + 1 = 1</td>
</tr>
</tbody>
</table>

In this lab, we will basic gates to implement a function.

Read the document about using breadboards:
http://faculty.unlv.edu/eelabs/docs/equipment/Breadboard.doc
LAB DELIVERIES:

PRELAB:

1. Create schematics in Quartus:
   Create a new project named ‘CPE100_LAB_2’ and add a new schematic to your project. On the schematic editor, create XOR schematic as shown on the Figure 1 using Altera Quartus software. Refer to the class website for the tutorials on using Altera Quartus.

   ![XOR gate diagram]

   Figure 1. XOR gate

2. Prelab deliveries
   Include in the report document:
   1. Schematics created in Quartus
   2. Simulation waveform generated by Quartus

LAB EXPERIMENTS:

1. Experiment 1: DC Power Supply Set Up with Multimeter
   Implement following Boolean equations using the 7400 series gates:
   a) $F = ab + a'b'$
   b) $F = ab + a'b$
   c) $F = (a+b)(a'+b')$
   d) $F = abc + a'b'c + a'cb$

   For each function do:
   1. Prepare truth table
   2. Test all combinations from truth table and verify, that your circuit yields the same results
   3. Demonstrate your verified circuit to TA

Note: in TTL which you use here, logic zero = 0V, logic one = +5V.
Steps to get circuit working – example for function a) $F = ab + a'b'$:
1. Split function into separate modules. For function a), there will be module $ab$ and module $a'b'$
2. Implement and test modules separately
3. Connect modules and test
4. It is possible, that the chip is faulty. To make sure the chip is working, connect +5V to VCC, 0V to GND, and connect one gate and test its operation.

Implementing $ab$ module:

Implement AND gate, and verify its operation by connecting the LED in series with 100Ω resistor

![Figure 2. Setup of AND gate with LED](image)

At this point, the $ab$ module is tested and working. Next step: implementing the $a'b'$ module. You need to invert the $a$ and $b$ signals first, using NOT gates.

![Figure 3. Setup of NOT and AND gate](image)
Now, having the \( ab \) and \( a'b' \) modules tested, you connect them using OR gate.

Place chip, and power it by connecting +5V to VCC, and 0V to GND. Connect \( a'b' \) and \( ab \), the output of OR gate is \( F \)

Figure 4. Connecting modules

Remember to have just single one wire for \( a \) signal, and just single one wire for \( b \) signal.

**POSTLAB REPORT:**

Include the following elements in the report document:

<table>
<thead>
<tr>
<th>Section</th>
<th>Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Theory of operation</td>
</tr>
<tr>
<td></td>
<td><em>Include a brief description of every element and phenomenon that appears during the experiments.</em></td>
</tr>
<tr>
<td>2</td>
<td>Prelab report</td>
</tr>
<tr>
<td>3</td>
<td>Results of the experiments</td>
</tr>
<tr>
<td></td>
<td><strong>Experiment</strong></td>
</tr>
<tr>
<td>4</td>
<td>Answer the questions</td>
</tr>
<tr>
<td></td>
<td><strong>Question no.</strong></td>
</tr>
<tr>
<td>5</td>
<td>Conclusions</td>
</tr>
<tr>
<td></td>
<td><em>Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.</em></td>
</tr>
<tr>
<td>6</td>
<td>Attachments</td>
</tr>
<tr>
<td></td>
<td><em>Zip your projects. Send through WebCampus as attachments, or provide link to the zip file on Google Drive / Dropbox, etc.</em></td>
</tr>
</tbody>
</table>

**List of attachments to deliver:**
1. XOR Quartus project
References:
2.Datasheets of 7400 series chips:
   http://faculty.unlv.edu/eelabs/index.html?navi=main_icdatasheets