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Contractor/manufacturer is:
Mentor Graphics Corporation
8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.
Telephone: 503.685.7000
Toll-Free Telephone: 800.592.2210
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Assumptions

We assume that you are familiar with the use of your operating system. You should also be familiar with the window management functions of your graphic interface: OpenWindows, OSF/Motif, CDE, KDE, GNOME, or Microsoft Windows 2000/XP.

We also assume that you have a working knowledge of the language in which your design and/or testbench is written (i.e., VHDL, Verilog, etc.). Although ModelSim™ is an excellent tool to use while learning HDL concepts and practices, this document is not written to support that goal.

Before you Begin

Preparation for some of the lessons leaves certain details up to you. You will decide the best way to create directories, copy files, and execute programs within your operating system. (When you are operating the simulator within ModelSim’s GUI, the interface is consistent for all platforms.)

Examples show Windows path separators - use separators appropriate for your operating system when trying the examples.

Example Designs

ModelSim comes with Verilog and VHDL versions of the designs used in these lessons. This allows you to do the tutorial regardless of which license type you have. Though we have tried to minimize the differences between the Verilog and VHDL versions, we could not do so in all cases. In cases where the designs differ (e.g., line numbers or syntax), you will find language-specific instructions. Follow the instructions that are appropriate for the language you use.
Chapter 2
Conceptual Overview

Introduction

ModelSim is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed-language designs.

This lesson provides a brief conceptual overview of the ModelSim simulation environment. It is divided into four topics, which you will learn more about in subsequent lessons.

- Basic simulation flow — Refer to Chapter 3 Basic Simulation.
- Project flow — Refer to Chapter 4 Projects.
- Multiple library flow — Refer to Chapter 5 Working With Multiple Libraries.
- Debugging tools — Refer to remaining lessons.

Basic Simulation Flow

The following diagram shows the basic steps for simulating a design in ModelSim.

Figure 2-1. Basic Simulation Flow - Overview Lab

- Creating the Working Library
In ModelSim, all designs are compiled into a library. You typically start a new simulation in ModelSim by creating a working library called "work". "Work" is the library name used by the compiler as the default destination for compiled design units.

- Compiling Your Design

After creating the working library, you compile your design units into it. The ModelSim library format is compatible across all supported platforms. You can simulate your design on any platform without having to recompile your design.

- Loading the Simulator with Your Design and Running the Simulation

With the design compiled, you load the simulator with your design by invoking the simulator on a top-level module (Verilog) or a configuration or entity/architecture pair (VHDL).

Assuming the design loads successfully, the simulation time is set to zero, and you enter a run command to begin simulation.

- Debugging Your Results

If you don’t get the results you expect, you can use ModelSim’s robust debugging environment to track down the cause of the problem.

Project Flow

A project is a collection mechanism for an HDL design under specification or test. Even though you don’t have to use projects in ModelSim, they may ease interaction with the tool and are useful for organizing files and specifying simulation settings.

The following diagram shows the basic steps for simulating a design within a ModelSim project.
Figure 2-2. Project Flow

Create a project

Add files to the project

Compile design files

Run simulation

Debug results

As you can see, the flow is similar to the basic simulation flow. However, there are two important differences:

- You do not have to create a working library in the project flow; it is done for you automatically.
- Projects are persistent. In other words, they will open every time you invoke ModelSim unless you specifically close them.

Multiple Library Flow

ModelSim uses libraries in two ways: 1) as a local working library that contains the compiled version of your design; 2) as a resource library. The contents of your working library will change as you update your design and recompile. A resource library is typically static and serves as a parts source for your design. You can create your own resource libraries, or they may be supplied by another design team or a third party (e.g., a silicon vendor).

You specify which resource libraries will be used when the design is compiled, and there are rules to specify in which order they are searched. A common example of using both a working library and a resource library is one where your gate-level design and testbench are compiled into the working library, and the design references gate-level models in a separate resource library.

The diagram below shows the basic steps for simulating with multiple libraries.
You can also link to resource libraries from within a project. If you are using a project, you would replace the first step above with these two steps: create the project and add the testbench to the project.

**Debugging Tools**

ModelSim offers numerous tools for debugging and analyzing your design. Several of these tools are covered in subsequent lessons, including:

- Using projects
- Working with multiple libraries
- Setting breakpoints and stepping through the source code
- Viewing waveforms and measuring time
- Viewing and initializing memories
- Creating stimulus with the Waveform Editor
- Automating simulation
Introduction

In this lesson you will go step-by-step through the basic simulation flow:

![Figure 3-1. Basic Simulation Flow - Simulation Lab](image)

Design Files for this Lesson

The sample design for this lesson is a simple 8-bit, binary up-counter with an associated testbench. The pathnames are as follows:

- **Verilog** – `<install_dir>/examples/tutorials/verilog/basicSimulation/counter.v` and `tcounter.v`
- **VHDL** – `<install_dir>/examples/tutorials/vhdl/basicSimulation/counter.vhd` and `tcounter.vhd`

This lesson uses the Verilog files `counter.v` and `tcounter.v`. If you have a VHDL license, use `counter.vhd` and `tcounter.vhd` instead. Or, if you have a mixed license, feel free to use the Verilog testbench with the VHDL counter or vice versa.

Related Reading


Create the Working Design Library

Before you can simulate a design, you must first create a library and compile the source code into that library.

1. Create a new directory and copy the design files for this lesson into it.
   
   Start by creating a new directory for this exercise (in case other users will be working with these lessons).

   **Verilog:** Copy `counter.v` and `tcounter.v` files from 
   `/<install_dir>/examples/tutorials/verilog/basicSimulation` to the new directory.

   **VHDL:** Copy `counter.vhd` and `tcounter.vhd` files from 
   `/<install_dir>/examples/tutorials/vhdl/basicSimulation` to the new directory.

2. Start ModelSim *if necessary.*
   
   a. Type `vsim` at a UNIX shell prompt or use the ModelSim icon in Windows.

      Upon opening ModelSim for the first time, you will see the Welcome to ModelSim dialog. Click **Close**.

   b. Select **File > Change Directory** and change to the directory you created in step 1.

3. Create the working library.
   
   a. Select **File > New > Library.**

      This opens a dialog where you specify physical and logical names for the library (Figure 3-2). You can create a new library or map to an existing library. We’ll be doing the former.

**Figure 3-2. The Create a New Library Dialog**

   ![Create a New Library Dialog](image)

   b. Type **work** in the Library Name field (if it isn’t already entered automatically).
c. Click OK.

ModelSim creates a directory called `work` and writes a specially-formatted file named `_info` into that directory. The `_info` file must remain in the directory to distinguish it as a ModelSim library. Do not edit the folder contents from your operating system; all changes should be made from within ModelSim.

ModelSim also adds the library to the list in the Workspace (Figure 3-3) and records the library mapping for future reference in the ModelSim initialization file (`modelsim.ini`).

![Figure 3-3. work Library in the Workspace](image)

When you pressed OK in step 3c above, the following was printed to the Transcript:

```plaintext
vlib work
vmap work work
```

These two lines are the command-line equivalents of the menu selections you made. Many command-line equivalents will echo their menu-driven functions in this fashion.

**Compile the Design**

With the working library created, you are ready to compile your source files.

You can compile by using the menus and dialogs of the graphic interface, as in the Verilog example below, or by entering a command at the ModelSim> prompt.

1. Compile `counter.v` and `tcounter.v`.
   a. Select Compile > Compile. This opens the Compile Source Files dialog (Figure 3-4).

   If the Compile menu option is not available, you probably have a project open. If so, close the project by making the Workspace pane active and selecting File > Close from the menus.
Create the Working Design Library

b. Select both `counter.v` and `tcounter.v` modules from the Compile Source Files dialog and click **Compile**. The files are compiled into the *work* library.

c. When compile is finished, click **Done**.

![Figure 3-4. Compile Source Files Dialog](image)

2. View the compiled design units.

   a. On the Library tab, click the `+` icon next to the *work* library and you will see two design units (**Figure 3-5**). You can also see their types (Modules, Entities, etc.) and the path to the underlying source files (scroll to the right if necessary).

![Figure 3-5. Verilog Modules Compiled into work Library](image)

**Load the Design**

1. Load the `test_counter` module into the simulator.

   a. In the Workspace, click the `+` sign next to the *work* library to show the files contained there.
b. Double-click *test_counter* to load the design.

You can also load the design by selecting **Simulate > Start Simulation** in the menu bar. This opens the Start Simulation dialog. With the Design tab selected, click the '+' sign next to the work library to see the *counter* and *test_counter* modules. Select the *test_counter* module and click OK (Figure 3-6).

![Start Simulation Dialog](image)

Figure 3-6. Loading Design with Start Simulation Dialog

When the design is loaded, you will see a new tab in the Workspace named *sim* that displays the hierarchical structure of the design (Figure 3-7). You can navigate within the hierarchy by clicking on any line with a '+' (expand) or '-' (contract) icon. You will also see a tab named *Files* that displays all files included in the design.
Basic Simulation
Run the Simulation

2. View design objects in the Objects pane.
   a. Open the View menu and select Objects. The command line equivalent is:

   ```
v view objects
   ```

   The Objects pane (Figure 3-8) shows the names and current values of data objects in the current region (selected in the Workspace). Data objects include signals, nets, registers, constants and variables not declared in a process, generics, parameters.

   **Figure 3-8. Object Pane Displays Design Objects**

   ![Object Pane](image)

   You may open other windows and panes with the View menu or with the `view` command. See Navigating the Interface.

Run the Simulation

Now you will open the Wave window, add signals to it, then run the simulation.

1. Open the Wave debugging window.
   a. Enter `view wave` at the command line.
You can also use the View > Wave menu selection to open a Wave window.

The Wave window is one of several windows available for debugging. To see a list of the other debugging windows, select the View menu. You may need to move or resize the windows to your liking. Window panes within the Main window can be zoomed to occupy the entire Main window or undocked to stand alone. For details, see Navigating the Interface.

2. Add signals to the Wave window.
   a. In the Workspace pane, select the sim tab.
   b. Right-click test_counter to open a popup context menu.
   c. Select Add > To Wave > All items in region (Figure 3-9).

   All signals in the design are added to the Wave window.

**Figure 3-9. Using the Popup Menu to Add Signals to Wave Window**

3. Run the simulation.
   a. Click the Run icon in the Main or Wave window toolbar.

The simulation runs for 100 ns (the default simulation length) and waves are drawn in the Wave window.

b. Enter run 500 at the VSIM> prompt in the Main window.

The simulation advances another 500 ns for a total of 600 ns (Figure 3-10).
Set Breakpoints and Step through the Source

Next you will take a brief look at one interactive debugging feature of the ModelSim environment. You will set a breakpoint in the Source window, run the simulation, and then step through the design under test. Breakpoints can be set only on lines with red line numbers.

1. Open `counter.v` in the Source window.
   a. Select the Files tab in the Main window Workspace.
   b. Click the + sign next to the sim filename to see the contents of vsim.wlf dataset.
   c. Double-click `counter.v` (or `counter.vhd` if you are simulating the VHDL files) to open it in the Source window.

2. Set a breakpoint on line 36 of `counter.v` (or, line 39 of `counter.vhd` for VHDL).
   a. Scroll to line 36 and click in the BP (breakpoint) column next to the line number. A red ball appears in the line number column at line number 36 (Figure 3-11), indicating that a breakpoint has been set.

   ![Figure 3-10. Waves Drawn in Wave Window](image)

   c. Click the Run -All icon on the Main or Wave window toolbar.

   The simulation continues running until you execute a break command or it hits a statement in your code (e.g., a Verilog $stop statement) that halts the simulation.

   d. Click the Break icon. The simulation stops running.
3. Disable, enable, and delete the breakpoint.
   a. Click the red ball to disable the breakpoint. It will become a black ball.
   b. Click the black ball again to re-enable the breakpoint. It will become a red ball.
   c. Click the red ball with your right mouse button and select **Remove Breakpoint 36**.
   d. Click in the line number column next to line number 36 again to re-create the breakpoint.

4. Restart the simulation.
   a. Click the Restart icon to reload the design elements and reset the simulation time to zero.

   The Restart dialog that appears gives you options on what to retain during the restart (Figure 3-12).
b. Click the **Restart** button in the Restart dialog.

c. Click the Run -All icon.

The simulation runs until the breakpoint is hit. When the simulation hits the breakpoint, it stops running, highlights the line with a blue arrow in the Source view (Figure 3-13), and issues a Break message in the Transcript pane.

**Figure 3-12. Setting Restart Functions**

![Restart dialog](image)

b. Click the **Restart** button in the Restart dialog.

c. Click the Run -All icon.

The simulation runs until the breakpoint is hit. When the simulation hits the breakpoint, it stops running, highlights the line with a blue arrow in the Source view (Figure 3-13), and issues a Break message in the Transcript pane.

**Figure 3-13. Blue Arrow Indicates Where Simulation Stopped.**

```
28  begin
29   increment[i] = val[i] ^ carry;
30   carry = val[i] & carry;
31  end
32  endfunction
34
35  always @ (posedge clk or posedge reset)
36    if (reset)
37      count = #tpd_reset_to_count 8'h00;
38    else
39    count <= #tpd_clk_to_count increment(count);
```

When a breakpoint is reached, typically you want to know one or more signal values. You have several options for checking values:

- look at the values shown in the Objects window (Figure 3-14).
Figure 3-14. Values Shown in Objects Window

- set your mouse pointer over a variable in the Source window and a yellow box will appear with the variable name and the value of that variable at the time of the selected cursor in the Wave window
- highlight a signal, parameter, or variable in the Source window, right-click it, and select Examine from the pop-up menu to display the variable and its current value in a Source Examine window (Figure 3-15)

Figure 3-15. Parameter Name and Value in Source Examine Window

- use the examine command at the VSIM> prompt to output a variable value to the Main window Transcript (i.e., examine count)

5. Try out the step commands.
   a. Click the Step icon on the Main window toolbar.

   This single-steps the debugger.

   Experiment on your own. Set and clear breakpoints and use the Step, Step Over, and Continue Run commands until you feel comfortable with their operation.

Navigating the Interface

The Main window is composed of a number of "panes" and sub-windows that display various types of information about your design, simulation, or debugging session. You can also access other tools from the Main window that display in stand-alone windows (e.g., the Dataflow window).
The following table describes some of the key elements of the Main window.

### Table 3-1. The Main Window

<table>
<thead>
<tr>
<th>Window/pane</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Workspace</td>
<td>This pane comprises multiple tabs that contain various sorts of information about the current project or design. Once a design is loaded, additional tabs will appear. Refer to the section <strong>Workspace</strong> in the User’s Manual for more information.</td>
</tr>
<tr>
<td>Transcript</td>
<td>The Transcript pane provides a command-line interface and serves as an activity log including status and error messages. Refer to the section <strong>Transcript Window</strong> in the User’s Manual for more information.</td>
</tr>
</tbody>
</table>
Here are a few important points to keep in mind about the ModelSim interface:

- Windows/panes can be resized, moved, zoomed, undocked, etc. and the changes are persistent.

You have a number of options for re-sizing, re-positioning, undocking/redocking, and generally modifying the physical characteristics of windows and panes. When you exit ModelSim, the current layout is saved so that it appears the same the next time you invoke the tool. Refer to the Main Window section in the User’s Manual for more information.

- Menus are context sensitive.

The menu items that are available and how certain menu items behave depend on which pane or window is active. For example, if the sim tab in the Workspace is active and you choose Edit from the menu bar, the Clear command is disabled. However, if you click in the Transcript pane and choose Edit, the Clear command is enabled. The active pane is denoted by a blue title bar.

Let us try a few things.

1. Zoom and undock panes.
   a. Click the Zoom/Unzoom icon in the upper right corner of the Workspace pane (Figure 3-17).

![Figure 3-17. Window/Pane Control Icons](image)

The pane fills the entire Main window (Figure 3-18).
b. Click the **Zoom/Unzoom pane** icon in the Workspace.

c. Click the **Dock/Undock pane** icon in the upper right corner of the Transcript pane. The Transcript becomes a stand-alone window.

d. Click the **Dock/Undock pane** icon on the Transcript.

e. Click the **Hide pane** icon in the Workspace.

f. Select **View > Workspace** from the menus to re-open the Workspace.

2. Move and resize panes.

   a. Hover your mouse pointer in the center of the Transcript title bar, where the two parallel lines are interrupted by 3 lines of small dots. This is the handle for the pane. When the cursor is over the pane handle it becomes a four-headed arrow. ![Four-headed arrow icon]

   b. Click and drag the Transcript up and to the right until you see a gray outline on the right-hand side of the MDI frame.

   When you let go of the mouse button, the Transcript is moved and the MDI frame and Workspace panes shift to the left (**Figure 3-19**).
c. Select **Layout > Reset**.

The layout returns to its original setting.

**Tip:** Moving panes can get confusing, and you may not always obtain the results you expect. Practice moving a pane around, watching the gray outline to see what happens when you drop it in various places. Your layout will be saved when you exit ModelSim and will reappear in the last configuration when you next open ModelSim. (It’s a good idea to close all panes in the MDI frame at the end of each lesson in this tutorial so only files relevant to each lesson will be displayed.)

As you practice, notice that the MDI frame cannot be moved in the same manner as the panes. It does not have a handle in its header bar.

Selecting **Layout > Reset** is the easiest way to rectify an undesired layout.

d. Hover your mouse pointer on the border between two panes so it becomes a double-headed arrow. 

e. Click-and-drag left and right or up and down to resize the pane.

f. Select **Layout > Reset**.

3. Observe context sensitivity of menu commands.

a. Click anywhere in the Workspace.

b. Select the Edit menu and notice that the **Clear** command is disabled.
Navigating the Interface

c. Click in the Transcript and select **Edit > Clear**.
   
   This command applies to the Transcript pane but not the Workspace pane.

d. Click on a design object in the sim tab of the Workspace and select **File > Open**.

e. Notice that the Open dialog filters to show Log files (*wlf).

f. Now click on a filename in the Files tab of the Workspace and select **File > Open**.
   
   Notice that the Open dialog filters to show HDL file types instead.

Lesson Wrap-Up

This concludes this lesson. Before continuing we need to end the current simulation.

1. Select **Simulate > End Simulation**.

2. Click **Yes** when prompted to confirm that you wish to quit simulating.
Introduction

In this lesson you will practice creating a project.

At a minimum, projects contain a work library and a session state that is stored in a .mpf file. A project may also consist of:

- HDL source files or references to source files
- other files such as READMEs or other project documentation
- local libraries
- references to global libraries

Design Files for this Lesson

The sample design for this lesson is a simple 8-bit, binary up-counter with an associated testbench. The pathnames are as follows:

Verilog – `<install_dir>/examples/tutorials/verilog/projects/counter.v` and `tcounter.v`

VHDL – `<install_dir>/examples/tutorials/vhdl/projects/counter.vhd` and `tcounter.vhd`

This lesson uses the Verilog files `tcounter.v` and `counter.v`. If you have a VHDL license, use `tcounter.vhd` and `counter.vhd` instead.

Related Reading


Create a New Project

1. Create a new directory and copy the design files for this lesson into it.

   Start by creating a new directory for this exercise (in case other users will be working with these lessons).

   **Verilog:** Copy `counter.v` and `tcounter.v` files from `/<install_dir>/examples/tutorials/verilog/projects` to the new directory.

   **VHDL:** Copy `counter.vhd` and `tcounter.vhd` files from `/<install_dir>/examples/tutorials/vhdl/projects` to the new directory.
2. If you just finished the previous lesson, ModelSim should already be running. If not, start ModelSim.
   a. Type `vsim` at a UNIX shell prompt or use the ModelSim icon in Windows.
   b. Select File > Change Directory and change to the directory you created in step 1.

3. Create a new project.
   a. Select File > New > Project (Main window) from the menu bar.
      This opens the Create Project dialog where you can enter a Project Name, Project Location (i.e., directory), and Default Library Name (Figure 4-1). You can also reference library settings from a selected .ini file or copy them directly into the project. The default library is where compiled design units will reside.
   b. Type `test` in the Project Name field.
   c. Click the Browse button for the Project Location field to select a directory where the project file will be stored.
   d. Leave the Default Library Name set to `work`.
   e. Click OK.

**Figure 4-1. Create Project Dialog - Project Lab**

![Create Project Dialog](image)

**Add Objects to the Project**

Once you click OK to accept the new project settings, you will see a blank Project tab in the Workspace area of the Main window and the Add items to the Project dialog will appear (Figure 4-2). From this dialog you can create a new design file, add an existing file, add a folder for organization purposes, or create a simulation configuration (discussed below).
1. Add two existing files.
   
a. Click **Add Existing File**.

   This opens the Add file to Project dialog (Figure 4-3). This dialog lets you browse to find files, specify the file type, specify a folder to which the file will be added, and identify whether to leave the file in its current location or to copy it to the project directory.

   **Figure 4-3. Add file to Project Dialog**

   ![Add file to Project Dialog](image)

   b. Click the **Browse** button for the File Name field. This opens the “Select files to add to project” dialog and displays the contents of the current directory.

   c. **Verilog**: Select `counter.v` and `tcounter.v` and click **Open**.

   **VHDL**: Select `counter.vhd` and `tcounter.vhd` and click **Open**.

   This closes the “Select files to add to project” dialog and displays the selected files in the “Add file to Project” dialog (Figure 4-3).

   d. Click **OK** to add the files to the project.
Projects

Create a New Project

e. Click **Close** to dismiss the Add items to the Project dialog.

You should now see two files listed in the Project tab of the Workspace pane (Figure 4-4). Question mark icons (?) in the Status column indicate that the file has not been compiled or that the source file has changed since the last successful compile. The other columns identify file type (e.g., Verilog or VHDL), compilation order, and modified date.

**Figure 4-4. Newly Added Project Files Display a “?” for Status**

<table>
<thead>
<tr>
<th>Name</th>
<th>Status</th>
<th>Type</th>
<th>Order</th>
<th>Modified</th>
</tr>
</thead>
<tbody>
<tr>
<td>counter.v</td>
<td>?</td>
<td>Verilog</td>
<td>1</td>
<td>10/26/06 08:47:58 PM</td>
</tr>
<tr>
<td>tcounter.v</td>
<td>?</td>
<td>Verilog</td>
<td>0</td>
<td>10/26/06 08:47:58 PM</td>
</tr>
</tbody>
</table>

**Changing Compile Order (VHDL)**

By default ModelSim performs default binding of VHDL designs when you load the design with **vsim**. However, you can elect to perform default binding at compile time. (For details, refer to the section **Default Binding** in the User’s Manual.) If you elect to do default binding at compile, then the compile order is important. Follow these steps to change compilation order within a project.

1. Change the compile order.

   a. Select **Compile > Compile Order**.

      This opens the Compile Order dialog box.

   b. Click the **Auto Generate** button.

      ModelSim "determines" the compile order by making multiple passes over the files. It starts compiling from the top; if a file fails to compile due to dependencies, it moves that file to the bottom and then recompiles it after compiling the rest of the files. It continues in this manner until all files compile successfully or until a file(s) can’t be compiled for reasons other than dependency.

      Alternatively, you can select a file and use the Move Up and Move Down buttons to put the files in the correct order (Figure 4-5).
c. Click OK to close the Compile Order dialog.

**Compile the Design**

1. Compile the files.
   
   a. Right-click either `counter.v` or `tcounder.v` in the Project tab and select **Compile > Compile All** from the pop-up menu.

   ModelSim compiles both files and changes the symbol in the Status column to a green check mark. A check mark means the compile succeeded. If compile fails, the symbol will be a red 'X', and you will see an error message in the Transcript pane.

2. View the design units.
   
   a. Click the **Library** tab in the workspace (**Figure 4-6**).

   b. Click the "+" icon next to the `work` library.

   You should see two compiled design units, their types (modules in this case), and the path to the underlying source files.
Load the Design

1. Load the test_counter design unit.
   a. Double-click the test_counter design unit.

You should see 3 new tabs in the Main window Workspace. The sim tab displays the structure of the test_counter design unit (Figure 4-7). The Files tab contains information about the underlying source files. The Memories tab lists all memories in the design.

At this point you would typically run the simulation and analyze or debug your design like you did in the previous lesson. For now, you’ll continue working with
the project. However, first you need to end the simulation that started when you loaded `test_counter`.

2. End the simulation.
   a. Select Simulate > End Simulation.
   b. Click Yes.

Organizing Projects with Folders

If you have a lot of files to add to a project, you may want to organize them in folders. You can create folders either before or after adding your files. If you create a folder before adding files, you can specify in which folder you want a file placed at the time you add the file (see Folder field in Figure 4-3). If you create a folder after adding files, you edit the file properties to move it to that folder.

Add Folders

As shown previously in Figure 4-2, the Add items to the Project dialog has an option for adding folders. If you have already closed that dialog, you can use a menu command to add a folder.

1. Add a new folder.
   a. Right-click inside the Projects tab of the Workspace and select Add to Project > Folder.
   b. Type Design Files in the Folder Name field (Figure 4-8).

   ![Figure 4-8. Adding New Folder to Project](image)

   c. Click OK.

   The new Design Files folder is displayed in the Project tab (Figure 4-9).
2. Add a sub-folder.
   a. Right-click anywhere in the Project tab and select Add to Project > Folder.
   b. Type HDL in the Folder Name field (Figure 4-10).
   c. Click the Folder Location drop-down arrow and select Design Files.
   d. Click OK.
      A ‘+’ icon appears next to the Design Files folder in the Project tab (Figure 4-11).
   e. Click the ‘+’ icon to see the HDL sub-folder.
Moving Files to Folders

If you don’t place files into a folder when you first add the files to the project, you can move them into a folder using the properties dialog.

1. Move tcounter.v and counter.v to the HDL folder.
   a. Select both counter.v and tcounter.v in the Project tab of the Workspace.
   b. Right-click either file and select Properties.
      This opens the Project Compiler Settings dialog (Figure 4-12), which allows you to set a variety of options on your design files.

   c. Click the Place In Folder drop-down arrow and select HDL.
   d. Click OK.

      The selected files are moved into the HDL folder. Click the ‘+’ icon next to the HDL folder to see the files.

      The files are now marked with a ‘?’ in the Status column because you moved the files. The project no longer knows if the previous compilation is still valid.

Simulation Configurations

A Simulation Configuration associates a design unit(s) and its simulation options. For example, let’s say that every time you load tcounter.v you want to set the simulator resolution to picoseconds (ps) and enable event order hazard checking. Ordinarily, you would have to specify those options each time you load the design. With a Simulation Configuration, you specify options for a design and then save a "configuration" that associates the design and its options.
Projects
Simulation Configurations

The configuration is then listed in the Project tab and you can double-click it to load tcounter.v along with its options.

1. Create a new Simulation Configuration.
   a. Right-click in the Projects tab and select **Add to Project > Simulation Configuration** from the popup menu.

   This opens the Add Simulation Configuration dialog (Figure 4-13). The tabs in this dialog present a myriad of simulation options. You may want to explore the tabs to see what is available. You can consult the ModelSim User’s Manual to get a description of each option.

   **Figure 4-13. Simulation Configuration Dialog**

   ![Simulation Configuration Dialog](image)

   b. Type **counter** in the **Simulation Configuration Name** field.
   c. Select **HDL** from the **Place in Folder** drop-down.
   d. Click the '+' icon next to the **work** library and select **test_counter**.
   e. Click the **Resolution** drop-down and select **ps**.
f. For Verilog, click the Verilog tab and check **Enable hazard checking (-hazards)**.

g. Click **Save**.

The Project tab now shows a Simulation Configuration named *counter* in the HDL folder (Figure 4-14).

![Figure 4-14. A Simulation Configuration in the Project Tab](image)

2. Load the Simulation Configuration.

   a. Double-click the *counter* Simulation Configuration in the Project tab.

   In the Transcript pane of the Main window, the `vsim` (the ModelSim simulator) invocation shows the `-hazards` and `-t ps` switches (Figure 4-15). These are the command-line equivalents of the options you specified in the Simulate dialog.

![Figure 4-15. Transcript Shows Options for Simulation Configurations](image)

**Lesson Wrap-Up**

This concludes this lesson. Before continuing you need to end the current simulation and close the current project.

1. Select **Simulate > End Simulation**. Click Yes.
Projects

Simulation Configurations

2. Select the Project tab in the Main window Workspace.
3. Right-click in this tab to open a popup menu and select Close Project.
4. Click OK.

If you do not close the project, it will open automatically the next time you start ModelSim.
Chapter 5
Working With Multiple Libraries

Introduction

In this lesson you will practice working with multiple libraries. You might have multiple libraries to organize your design, to access IP from a third-party source, or to share common parts between simulations.

You will start the lesson by creating a resource library that contains the counter design unit. Next, you will create a project and compile the testbench into it. Finally, you will link to the library containing the counter and then run the simulation.

Design Files for this Lesson

The sample design for this lesson is a simple 8-bit, binary up-counter with an associated testbench. The pathnames are as follows:

Verilog – <install_dir>/examples/tutorials/verilog/libraries/counter.v and tcounter.v

VHDL – <install_dir>/examples/tutorials/vhdl/libraries/counter.vhd and tcounter.vhd

This lesson uses the Verilog files tcounter.v and counter.v in the examples. If you have a VHDL license, use tcounter.vhd and counter.vhd instead.

Related Reading


Creating the Resource Library

Before creating the resource library, make sure the modelsim.ini in your install directory is “Read Only.” This will prevent permanent mapping of resource libraries to the master modelsim.ini file. See Permanently Mapping VHDL Resource Libraries.

1. Create a directory for the resource library.
   Create a new directory called resource_library. Copy counter.v from <install_dir>/examples/tutorials/verilog/libraries to the new directory.

2. Create a directory for the testbench.
Create a new directory called testbench that will hold the testbench and project files. Copy tcounter.v from <install_dir>/examples/tutorials/verilog/libraries to the new directory.

You are creating two directories in this lesson to mimic the situation where you receive a resource library from a third-party. As noted earlier, we will link to the resource library in the first directory later in the lesson.

3. Start ModelSim and change to the resource_library directory.
   If you just finished the previous lesson, ModelSim should already be running. If not, start ModelSim.
   a. Type vsim at a UNIX shell prompt or use the ModelSim icon in Windows.
      If the Welcome to ModelSim dialog appears, click Close.
   b. Select File > Change Directory and change to the resource_library directory you created in step 1.

4. Create the resource library.
   a. Select File > New > Library.
   b. Type parts_lib in the Library Name field (Figure 5-1).

   **Figure 5-1. Creating New Resource Library**

   ![Create a New Library dialog box]

   The Library Physical Name field is filled out automatically.
   Once you click OK, ModelSim creates a directory for the library, lists it in the Library tab of the Workspace, and modifies the modelsim.ini file to record this new library for the future.

5. Compile the counter into the resource library.
a. Click the Compile icon on the Main window toolbar.

b. Select the parts_lib library from the Library list (Figure 5-2).

c. Double-click counter.v to compile it.

d. Click Done.

You now have a resource library containing a compiled version of the counter design unit.

6. Change to the testbench directory.

a. Select File > Change Directory and change to the testbench directory you created in step 2.

Creating the Project

Now you will create a project that contains tcouter.v, the counter’s testbench.

1. Create the project.

a. Select File > New > Project.

b. Type counter in the Project Name field.

c. Do not change the Project Location field or the Default Library Name field. (The default library name is work.)
d. Make sure “Copy Library Mappings” is selected. The default modelsim.ini file will be used.

   e. Click OK.

2. Add the testbench to the project.
   a. Click Add Existing File in the Add items to the Project dialog.
   b. Click the Browse button and select tc0unter.v in the “Select files to add to project” dialog.
   c. Click Open.
   d. Click OK.
   e. Click Close to dismiss the “Add items to the Project” dialog.

   The tc0unter.v file is listed in the Project tab of the Main window.

3. Compile the testbench.
   a. Right-click tc0unter.v and select Compile > Compile Selected.

**Linking to the Resource Library**

To wrap up this part of the lesson, you will link to the parts_lib library you created earlier. But first, try simulating the testbench without the link and see what happens.

ModelSim responds differently for Verilog and VHDL in this situation.

**Verilog**

1. Simulate a Verilog design with a missing resource library.
   a. In the Library tab, click the ’+’ icon next to the work library and double-click test_counter.

   The Main window Transcript reports an error (Figure 5-3). When you see a message that contains text like "Error: (vsim-3033)", you can view more detail by using the verror command.
Working With Multiple Libraries

Linking to the Resource Library

Figure 5-3. Verilog Simulation Error Reported in Main Window

```
ModelSim> vsim work.test_counter
# vsim work.test_counter
# Loading work.test_counter
# ** Error: (vsim-3033) C:\Tutorials\examples\tutorials\verilog\libraries\testbench\tcounter.v(15): Instantiation of 'counter' failed. The design unit was not found.
# Region: /test_counter
# Search libraries:
# C:\Tutorials\examples\tutorials\verilog\libraries\testbench\work
# Error loading design

ModelSim>
```

b. Type `verror 3033` at the ModelSim> prompt.

The expanded error message tells you that a design unit could not be found for instantiation. It also tells you that the original error message should list which libraries ModelSim searched. In this case, the original message says ModelSim searched only `work`.

VHDL

1. Simulate a VHDL design with a missing resource library.

   a. In the Library tab, click the '+' icon next to the `work` library and double-click `test_counter`.

   The Main window Transcript reports a warning (Figure 5-4). When you see a message that contains text like "Warning: (vsim-3473)", you can view more detail by using the `verror` command.

Figure 5-4. VHDL Simulation Warning Reported in Main Window

```
# vsim -voptargs="-acc\" test_counter
# ** Note: (vsim-3812) Design is being optimized...
# ** Warning: [1] (vopt-3473) Component instance "dut : counter" is not bound.
# Loading C:\QuestaSim_E.2e_Beta\win32\../std.standard
# Loading work.test_counter(only)
# ** Warning: (vsim-3473) Component instance "dut : counter" is not bound.
# Time: 0 ns  Iteration: 0  Region: /test_counter  File: C:\Tutorials\examples\tutorials\vhdl\libraries\testbench\tcounter.vhd
```

b. Type `verror 3473` at the VSIM> prompt.
The expanded error message tells you that a component ('dut' in this case) has not been explicitly bound and no default binding can be found.

c. Type `quit -sim` to quit the simulation.

The process for linking to a resource library differs between Verilog and VHDL. If you are using Verilog, follow the steps in Linking in Verilog. If you are using VHDL, follow the steps in Linking in VHDL one page later.

### Linking in Verilog

Linking in Verilog requires that you specify a "search library" when you invoke the simulator.

1. Specify a search library during simulation.
   a. Click the Simulate icon on the Main window toolbar.
   b. Click the ‘+’ icon next to the `work` library and select `test_counter`.
   c. Click the Libraries tab.
   d. Click the Add button next to the Search Libraries field and browse to `parts_lib` in the `resource_library` directory you created earlier in the lesson.
   e. Click OK.
      The dialog should have `parts_lib` listed in the Search Libraries field (Figure 5-5).
   f. Click OK.
      The design loads without errors.
Linking in VHDL

To link to a resource library in VHDL, you have to create a logical mapping to the physical library and then add LIBRARY and USE statements to the source file.

1. Create a logical mapping to `parts_lib`.
   a. Select **File > New > Library**.
   b. In the Create a New Library dialog, select **a map to an existing library**.
   c. Type `parts_lib` in the Library Name field.
   d. Click Browse to open the Browse for Folder dialog and browse to `parts_lib` in the `resource_library` directory you created earlier in the lesson.
   e. Click OK to select the library and close the Select Library dialog.
   f. The Create a New Library dialog should look similar to the one shown in **Figure 5-6**. Click **OK** to close the dialog.
Figure 5-6. Mapping to the parts_lib Library

2. Add LIBRARY and USE statements to `tcounter.vhd`.
   a. In the Library tab of the Main window, click the ‘+’ icon next to the work library.
   b. Right-click `test_counter` in the work library and select Edit.
   c. This opens the file in the Source window.
   d. Right-click in the Source window and uncheck Read Only.
   e. Add these two lines to the top of the file:

```
LIBRARY parts_lib;
USE parts_lib.ALL;
```

The testbench source code should now look similar to that shown in Figure 5-7.

f. Select File > Save.
Permanently Mapping VHDL Resource Libraries

If you reference particular VHDL resource libraries in every VHDL project or simulation, you may want to permanently map the libraries. Doing this requires that you edit the master `modelsim.ini` file in the installation directory. Though you won’t actually practice it in this tutorial, here are the steps for editing the file:

1. Locate the `modelsim.ini` file in the ModelSim installation directory (<install_dir>/modeltech/modelsim.ini).
2. IMPORTANT - Make a backup copy of the file.
3. Change the file attributes of `modelsim.ini` so it is no longer "read-only."
4. Open the file and enter your library mappings in the [Library] section. For example:
   
   ```
   parts_lib = C:/libraries/parts_lib
   ```
5. Save the file.
6. Change the file attributes so the file is "read-only" again.

Lesson Wrap-Up

This concludes this lesson. Before continuing we need to end the current simulation and close the project.

1. Select Simulate > End Simulation. Click Yes.
2. Select the Project tab of the Main window Workspace.
3. Select File > Close. Click OK.
Introduction

The Wave window allows you to view the results of your simulation as HDL waveforms and their values. The Wave window is divided into a number of panes (Figure 6-1). You can resize the pathnames pane, the values pane, and the waveform pane by clicking and dragging the bar between any two panes.
Related Reading

User’s Manual sections: Wave Window and Recording Simulation Results With Datasets

Loading a Design

For the examples in this lesson, we have used the design simulated in Basic Simulation.

1. If you just finished the previous lesson, ModelSim should already be running. If not, start ModelSim.
   a. Type `vsim` at a UNIX shell prompt or use the ModelSim icon in Windows.
      If the Welcome to ModelSim dialog appears, click Close.

2. Load the design.
   a. Select File > Change Directory and open the directory you created in the “Basic Simulation” lesson.
      The `work` library should already exist.
   b. Click the ‘+’ icon next to the `work` library and double-click `test_counter`.
      ModelSim loads the design and adds `sim` and `Files` tabs to the Workspace.

Add Objects to the Wave Window

ModelSim offers several methods for adding objects to the Wave window. In this exercise, you will try different methods.

1. Add objects from the Objects pane.
   a. Select an item in the Objects pane of the Main window, right-click, and then select Add > To Wave > All items in region.
      ModelSim adds several signals to the Wave window.

2. Undock the Wave window.
   By default ModelSim opens Wave windows as a tab in the MDI frame of the Main window. You can change the default via the Preferences dialog (Tools > Edit Preferences). Refer to the section Simulator GUI Preferences in the User’s Manual for more information.
   a. Click the undock button on the Wave pane (Figure 6-2).
      The Wave pane becomes a standalone, un-docked window. You may need to resize the window.

You can drag an object to the Wave window from many other windows and panes (e.g., Workspace, Objects, and Locals).

a. In the Wave window, select Edit > Select All and then Edit > Delete.

b. Drag an instance from the sim tab of the Main window to the Wave window.

ModelSim adds the objects for that instance to the Wave window.

c. Drag a signal from the Objects pane to the Wave window.

d. In the Wave window, select Edit > Select All and then Edit > Delete.

4. Add objects using a command.

a. Type add wave * at the VSIM> prompt.

ModelSim adds all objects from the current region.

b. Run the simulation for awhile so you can see waveforms.

**Zooming the Waveform Display**

Zooming lets you change the display range in the waveform pane. There are numerous methods for zooming the display.

1. Zoom the display using various techniques.

a. Click the Zoom Mode icon on the Wave window toolbar.

b. In the waveform pane, click and drag down and to the right.
You should see blue vertical lines and numbers defining an area to zoom in (Figure 6-3).

**Figure 6-3. Zooming in with the Mouse Pointer**

![Zooming in with the Mouse Pointer](image)

c. Select **View > Zoom > Zoom Last**.

The waveform pane returns to the previous display range.

d. Click the Zoom In 2x icon a few times.

e. In the waveform pane, click and drag up and to the right.

You should see a blue line and numbers defining an area to zoom out.

f. Select **View > Zoom > Zoom Full**.

### Using Cursors in the Wave Window

Cursors mark simulation time in the Wave window. When ModelSim first draws the Wave window, it places one cursor at time zero. Clicking anywhere in the waveform pane brings that cursor to the mouse location.

You can also add additional cursors; name, lock, and delete cursors; use cursors to measure time intervals; and use cursors to find transitions.

First, dock the Wave window in the Main window by clicking the dock icon.

### Working with a Single Cursor

1. Position the cursor by clicking and dragging.
   
   a. Click the Select Mode icon on the Wave window toolbar.
   
   b. Click anywhere in the waveform pane.
A cursor is inserted at the time where you clicked (Figure 6-4).

**Figure 6-4. Working with a Single Cursor in the Wave Window**

![Waveform Window with Cursor](image)

c. Drag the cursor and observe the value pane.

   The signal values change as you move the cursor. This is perhaps the easiest way to examine the value of a signal at a particular time.

d. In the waveform pane, drag the cursor to the right of a transition with the mouse positioned over a waveform.

   The cursor "snaps" to the nearest transition to the left. Cursors "snap" to a waveform edge if you click or drag a cursor to within ten pixels of a waveform edge. You can set the snap distance in the Window Preferences dialog (select **Tools > Window Preferences**).

e. In the cursor pane, drag the cursor to the right of a transition (Figure 6-4).

   The cursor doesn’t snap to a transition if you drag in the cursor pane.

2. Rename the cursor.

   a. Right-click "Cursor 1" in the cursor name pane, and select and delete the text.

   b. Type **A** and press Enter.

      The cursor name changes to "A" (Figure 6-5).
3. Jump the cursor to the next or previous transition.
   a. Click signal *count* in the pathname pane.
   b. Click the Find Next Transition icon on the Wave window toolbar.
      The cursor jumps to the next transition on the currently selected signal.
   c. Click the Find Previous Transition icon on the Wave window toolbar.
      The cursor jumps to the previous transition on the currently selected signal.

**Working with Multiple Cursors**

1. Add a second cursor.
   a. Click the Add Cursor icon on the Wave window toolbar.
   b. Right-click the name of the new cursor and delete the text.
   c. Type *B* and press Enter.
   d. Drag cursor *B* and watch the interval measurement change dynamically (Figure 6-6).
Figure 6-6. Interval Measurement Between Two Cursors

2. Lock cursor B.
   a. Right-click cursor B in the cursor pane and select Lock B.

   The cursor color changes to red and you can no longer drag the cursor (Figure 6-7).

Figure 6-7. A Locked Cursor in the Wave Window

3. Delete cursor B.
   a. Right-click cursor B and select Delete B.

Lesson Wrap-Up

This concludes this lesson. Before continuing we need to end the current simulation.

1. Select Simulate > End Simulation. Click Yes.
Analyzing Waveforms

Using Cursors in the Wave Window
Chapter 7
Viewing And Initializing Memories

Introduction

In this lesson you will learn how to view and initialize memories in . defines and lists as memories any of the following:

- reg, wire, and std_logic arrays
- Integer arrays
- Single dimensional arrays of VHDL enumerated types other than std_logic

Design Files for this Lesson

The installation comes with Verilog and VHDL versions of the example design. The files are located in the following directories:

This lesson uses the Verilog version for the exercises. If you have a VHDL license, use the VHDL version instead.

Related Reading

User’s Manual Section: Memory Panes.

Reference Manul commands: mem display, mem load, mem save, and radix.

Compile and Load the Design

1. Create a new directory and copy the tutorial files into it.

   Start by creating a new directory for this exercise (in case other users will be working with these lessons). Create the directory and copy all files from <install_dir>/examples/tutorials/verilog/memory to the new directory.

   If you have a VHDL license, copy the files in <install_dir>/examples/tutorials/vhdl/memory instead.

2. Start ModelSim and change to the exercise directory.

   If you just finished the previous lesson, ModelSim should already be running. If not, start ModelSim.

   a. Type vsim at a UNIX shell prompt or use the ModelSim icon in Windows.

      If the Welcome to ModelSim dialog appears, click Close.
b. Select *File > Change Directory* and change to the directory you created in step 1.

3. Create the working library and compile the design.
   a. Type `vlib work` at the ModelSim> prompt.
   b. **Verilog:**
      Type `vlog sp_syn_ram.v dp_syn_ram.v ram_tb.v` at the ModelSim> prompt.
   
   **VHDL:**
   Type `vcom -93 sp_syn_ram.vhd dp_syn_ram.vhd ram_tb.vhd` at the ModelSim> prompt.

4. Load the design.
   a. On the Library tab of the Main window Workspace, click the "+" icon next to the `work` library.
   b. Double-click the `ram_tb` design unit to load the design.

**View a Memory and its Contents**

The Memories tab of the Main window lists all memories in the design (*Figure 7-1*) when the design is loaded; with the range, depth, and width of each memory displayed.

*Figure 7-1. Viewing the Memories Tab in the Main Window Workspace*

 VHDL: The radix for enumerated types is Symbolic. To change the radix to binary for the purposes of this lesson, type the following command at the VSIM> prompt:

```
radix bin
```

1. Open a Memory instance to show its contents.
   a. Double-click the `/ram_tb/spram1/mem` instance in the memories list to view its contents in the MDI frame.

A *mem* tab is created in the MDI frame to display the memory contents. The data are all X (0 in VHDL) since you have not yet simulated the design. The first column
blue hex characters) lists the addresses (Figure 7-2), and the remaining columns show the data values.

Figure 7-2. The mem Tab in the MDI Frame Shows Addresses and Data

b. Double-click instance /ram_tb/spram2/mem in the Memories tab of the Workspace, This creates a new tab in the MDI frame called mem(1) that contains the addresses and data for the spram2 instance. Each time you double-click a new memory instance in the Workspace, a new tab is created for that instance in the MDI frame.

2. Simulate the design.

a. Click the run -all icon in the Main window.

b. Click the mem tab of the MDI frame to bring the /ram_tb/spram1/mem to the foreground. The data fields now show values (Figure 7-3).

Figure 7-3. The Memory Display Updates with the Simulation

VHDL:
In the Transcript pane, you will see NUMERIC_STD warnings that can be ignored and
an assertion failure that is functioning to stop the simulation. The simulation itself has not failed.

3. Change the address radix and the number of words per line for instance /ram_tb/spram1/mem.

a. Right-click anywhere in the Memory Contents pane and select Properties.

b. The Properties dialog box opens (Figure 7-4).

c. For the **Address Radix**, select **Decimal**. This changes the radix for the addresses only.

d. Select **Words per line** and type 1 in the field.

e. Click OK.

You can see the results of the settings in Figure 7-5. If the figure doesn’t match what you have in your ModelSim session, check to make sure you set the Address Radix rather than the Data Radix. Data Radix should still be set to Symbolic, the default.
Viewing And Initializing Memories

View a Memory and its Contents

Navigate Within the Memory

You can navigate to specific memory address locations, or to locations containing particular data patterns. First, you will go to a specific address.

1. Use Goto to find a specific address.
   a. Right-click anywhere in address column and select Goto (Figure 7-6).
      The Goto dialog box opens in the data pane.

      Figure 7-6. Goto Dialog

      b. Type 30 in the Goto Address field.
      c. Click OK.
         The requested address appears in the top line of the window.

2. Edit the address location directly.
a. To quickly move to a particular address, do the following:
   i. Double click address 38 in the address column.
   ii. Enter address 100 (Figure 7-7).

   **Figure 7-7. Editing the Address Directly**

   iii. Press <Enter> on your keyboard.

   The pane scrolls to that address.

3. Now, let’s find a particular data entry.
   a. Right-click anywhere in the data column and select **Find**.

   The Find in dialog box opens (Figure 7-8).

   **Figure 7-8. Searching for a Specific Data Value**
b. Type 1111010 in the **Find data** field and click **Find Next**.

   The data scrolls to the first occurrence of that address. Click **Find Next** a few more times to search through the list.

   c. Click **Close** to close the dialog box.

### Export Memory Data to a File

You can save memory data to a file that can be loaded at some later point in simulation.

1. Export a memory pattern from the `/ram_tb/spram1/mem` instance to a file.
   a. Make sure `/ram_tb/spram1/mem` is open and selected in the MDI frame.
   b. Select **File > Export > Memory Data** to bring up the Export Memory dialog box (Figure 7-9).
Export Memory Data to a File

Viewing And Initializing Memories

Figure 7-9. Export Memory Dialog

- For the Address Radix, select **Decimal**.
- For the Data Radix, select **Binary**.
- For the Line Wrap, set to 1 word per line.
- Type **data_mem.mem** into the Filename field.
- Click OK.

You can view the exported file in any editor.

Memory pattern files can be exported as relocatable files, simply by leaving out the address information. Relocatable memory files can be loaded anywhere in a memory because no addresses are specified.
2. Export a relocatable memory pattern file from the \texttt{/ram\_tb/spram2/mem} instance.
   a. Select the \texttt{mem(1)} tab in the MDI pane to see the data for the \texttt{/ram\_tb/spram2/mem} instance.
   b. Right-click on the memory contents to open a popup menu and select \textbf{Properties}.
   c. In the Properties dialog, set the Address Radix to \textbf{Decimal}; the Data Radix to \textbf{Binary}; and the Line Wrap to 1 \textbf{Words per Line}. Click OK to accept the changes and close the dialog.
   d. Select \textbf{File} > \textbf{Export} > \textbf{Memory Data} to bring up the Export Memory dialog box.
   e. For the Address Range, specify a Start address of 0 and End address of 250.
   f. For the File Format, select \textbf{MTI} and click \textbf{No addresses} to create a memory pattern that you can use to relocate somewhere else in the memory, or in another memory.
   g. For Address Radix select \textbf{Decimal}, and for Data Radix select \textbf{Binary}.
   h. For the Line Wrap, set 1 \textbf{Words per Line}.
   i. Enter the file name as \texttt{reloc.mem}, then click OK to save the memory contents and close the dialog. You will use this file for initialization in the next section.

\textbf{Initialize a Memory}

In ModelSim, it is possible to initialize a memory using one of three methods: from an exported memory file, from a fill pattern, or from both.

First, let’s initialize a memory from a file only. You will use one you exported previously, \texttt{data\_mem.mem}.

1. View instance \texttt{/ram\_tb/spram3/mem}.
   a. Double-click the \texttt{/ram\_tb/spram3/mem} instance in the Memories tab.
   This will open a new tab – \texttt{mem(2)} – in the MDI frame to display the contents of \texttt{/ram\_tb/spram3/mem}. Scan these contents so you can identify changes once the initialization is complete.
   b. Right-click and select \textbf{Properties} to bring up the Properties dialog.
   c. Change the Address Radix to \textbf{Decimal}, Data Radix to \textbf{Binary}, \textbf{Line Wrap to 1 Words per Line}, and click OK.

2. Initialize \texttt{spram3} from a file.
   a. Right-click anywhere in the data column and select \textbf{Import} to bring up the Import Memory dialog box (Figure 7-10).
The default Load Type is File Only.

b. Type *data_mem.mem* in the Filename field.

c. Click **OK**.

The addresses in instance */ram_tb/spram3/mem* are updated with the data from *data_mem.mem* ([Figure 7-11]).
In this next step, you will experiment with importing from both a file and a fill pattern. You will initialize spram3 with the 250 addresses of data you exported previously into the relocatable file reloc.mem. You will also initialize 50 additional address entries with a fill pattern.

3. Import the /ram_tb/spram3/mem instance with a relocatable memory pattern (reloc.mem) and a fill pattern.
   a. Right-click in the data column of the mem(2) tab and select Import to bring up the Import Memory dialog box.
   b. For Load Type, select Both File and Data.
   c. For Address Range, select Addresses and enter 0 as the Start address and 300 as the End address.
      This means that you will be loading the file from 0 to 300. However, the reloc.mem file contains only 251 addresses of data. Addresses 251 to 300 will be loaded with the fill data you specify next.
   d. For File Load, select the MTI File Format and enter reloc.mem in the Filename field.
   e. For Data Load, select a Fill Type of Increment.
   f. In the Fill Data field, set the seed value of 0 for the incrementing data.
   g. Click OK.
   h. View the data near address 250 by double-clicking on any address in the Address column and entering 250.

You can see the specified range of addresses overwritten with the new data. Also, you can see the incrementing data beginning at address 251 (Figure 7-12).
4. Right-click somewhere in the mem(2) pane and select **Close All**.

**Interactive Debugging Commands**

The memory panes can also be used interactively for a variety of debugging purposes. The features described in this section are useful for this purpose.

1. Open a memory instance and change its display characteristics.
   b. Right-click in the memory contents pane and select **Properties**.
   c. Change the Address and Data Radix to **Hexadecimal**.
   d. Select **Words per line** and enter 2.
   e. Click **OK**. The result should be as in **Figure 7-13**.
2. Initialize a range of memory addresses from a fill pattern.
   a. Right-click in the data column of /ram_tb/dpram1/mem contents pane and select Change to open the Change Memory dialog (Figure 7-14).

   **Figure 7-14. Changing Memory Content for a Range of Addresses**

   ![Change Memory Dialog](image)

   b. Select Addresses and enter the start address as **0x00000006** and the end address as **0x00000009**. The "0x" hex notation is optional.
   
   c. Select Random as the Fill Type.
   
   d. Enter 0 as the Fill Data, setting the seed for the Random pattern.
   
   e. Click OK.

   The data in the specified range are replaced with a generated random fill pattern (Figure 7-15).
Figure 7-15. Random Content Generated for a Range of Addresses

![Image of memory window with random content]

3. Change contents by highlighting.
   
   You can also change data by highlighting them in the Address Data pane.

   a. Highlight the data for the addresses `0x0000000c:0x0000000e`, as shown in Figure 7-16.

   ![Image of memory window with highlighted data]

   Figure 7-16. Changing Memory Contents by Highlighting

   b. Right-click the highlighted data and select **Change**.

   This brings up the Change memory dialog box (Figure 7-17). Note that the Addresses field is already populated with the range you highlighted.
c. Select **Value** as the Fill Type.

d. Enter the data values into the Fill Data field as follows: **34 35 36**

e. Click **OK**.

The data in the address locations change to the values you entered (Figure 7-18).

**Figure 7-18. Changed Memory Contents for the Specified Addresses**

4. **Edit data in place.**

To edit only one value at a time, do the following:

a. Double click any value in the Data column.

b. Enter the desired value and press <Enter> on your keyboard.

If you needed to cancel the edit function, press the <Esc> key on your keyboard.
Lesson Wrap-Up

This concludes this lesson. Before continuing we need to end the current simulation.

1. Select Simulate > End Simulation. Click Yes.
Chapter 8
Automating Simulation

Introduction

Aside from executing a couple of pre-existing DO files, the previous lessons focused on using ModelSim in interactive mode: executing single commands, one after another, via the GUI menus or Main window command line. In situations where you have repetitive tasks to complete, you can increase your productivity with DO files.

DO files are scripts that allow you to execute many commands at once. The scripts can be as simple as a series of ModelSim commands with associated arguments, or they can be full-blown Tcl programs with variables, conditional execution, and so forth. You can execute DO files from within the GUI or you can run them from the system command prompt without ever invoking the GUI.

Note

This lesson assumes that you have added the <install_dir>/modeltech/<platform> directory to your PATH. If you did not, you will need to specify full paths to the tools (i.e., vlib, vmap, vlog, vcom, and vsim) that are used in the lesson.

Related Reading

User’s Manual Chapter: Tcl and Macros (DO Files).

Practical Programming in Tcl and Tk, Brent B. Welch, Copyright 1997

Creating a Simple DO File

Creating DO files is as simple as typing the commands in a text file. Alternatively, you can save the Main window transcript as a DO file. In this exercise, you will use the commands you enter in the Main window transcript to create a DO file that adds signals to the Wave window, provides stimulus to those signals, and then advances the simulation.

1. Load the test_counter design unit.
   a. If necessary, start ModelSim.
   b. Change to the directory you created in the "Basic Simulation" lesson.
   c. Enter vsim test_counter to load the design unit.
2. Enter commands to add signals to the Wave window, force signals, and run the simulation.
   a. Select File > New > Source > Do to create a new DO file.
   b. Enter the following commands into the source window:
      
      ```
      add wave count
      add wave clk
      add wave reset
      force -freeze clk 0 0, 1 {50 ns} -r 100
      force reset 1
      run 100
      force reset 0
      run 300
      force reset 1
      run 400
      force reset 0
      run 200
      ```

3. Save the file.
   a. Select File > Save As.
   b. Type sim.do in the File name: field and save it to the current directory.

4. Load the simulation again and use the DO file.
   a. Enter quit -sim at the VSIM> prompt.
   b. Enter vsim test_counter at the ModelSim> prompt.
   c. Enter do sim.do at the VSIM> prompt.

      ModelSim executes the saved commands and draws the waves in the Wave window.

5. When you are done with this exercise, select File > Quit to quit ModelSim.

Running in Command-Line Mode

We use the term "command-line mode" to refer to simulations that are run from a DOS/UNIX prompt without invoking the GUI. Several ModelSim commands (e.g., vsim, vlib, vlog, etc.) are actually stand-alone executables that can be invoked at the system command prompt. Additionally, you can create a DO file that contains other ModelSim commands and specify that file when you invoke the simulator.

1. Create a new directory and copy the tutorial files into it.

   Start by creating a new directory for this exercise. Create the directory and copy the following files into it:
   
   - `/<install_dir>/examples/tutorials/verilog/automation/counter.v`
   - `/<install_dir>/examples/tutorials/verilog/automation/stim.do`
This lesson uses the Verilog file `counter.v`. If you have a VHDL license, use the `counter.vhd` and `stim.do` files in the `/<install_dir>/examples/tutorials/vhdl/automation` directory instead.

2. Create a new design library and compile the source file.

   Again, enter these commands at a DOS/UNIX prompt in the new directory you created in step 1.

   a. Type `vlib work` at the DOS/UNIX prompt.

   b. For Verilog, type `vlog counter.v` at the DOS/UNIX prompt. For VHDL, type `vcom counter.vhd`.

3. Create a DO file.

   a. Open a text editor.

   b. Type the following lines into a new file:

   ```
   # list all signals in decimal format
   add list -decimal *

   # read in stimulus
   do stim.do

   # output results
   write list counter.lst

   # quit the simulation
   quit -f
   ```

   c. Save the file with the name `sim.do` and place it in the current directory.

4. Run the batch-mode simulation.

   a. Type `vsim -c -do sim.do counter -wlf counter.wlf` at the DOS/UNIX prompt.

      The `-c` argument instructs ModelSim not to invoke the GUI. The `-wlf` argument saves the simulation results in a WLF file. This allows you to view the simulation results in the GUI for debugging purposes.

5. View the list output.

   a. Open `counter.lst` and view the simulation results. Output produced by the Verilog version of the design should look like the following:
### Automating Simulation

#### Running in Command-Line Mode

<table>
<thead>
<tr>
<th>ns</th>
<th>/counter/count</th>
</tr>
</thead>
<tbody>
<tr>
<td>delta</td>
<td>/counter/clk</td>
</tr>
<tr>
<td></td>
<td>/counter/reset</td>
</tr>
<tr>
<td>0</td>
<td>+0</td>
</tr>
<tr>
<td>1</td>
<td>+0</td>
</tr>
<tr>
<td>50</td>
<td>+0</td>
</tr>
<tr>
<td>100</td>
<td>+0</td>
</tr>
<tr>
<td>100</td>
<td>+1</td>
</tr>
<tr>
<td>150</td>
<td>+0</td>
</tr>
<tr>
<td>151</td>
<td>+0</td>
</tr>
<tr>
<td>200</td>
<td>+0</td>
</tr>
<tr>
<td>250</td>
<td>+0</td>
</tr>
</tbody>
</table>

The output may appear slightly different if you used the VHDL version.

6. View the results in the GUI.

   Since you saved the simulation results in `counter.wlf`, you can view them in the GUI by invoking VSIM with the `-view` argument.

**Note**

Make sure your PATH environment variable is set with the current version of ModelSim at the front of the string.

a. Type `vsim -view counter.wlf` at the DOS/UNIX prompt.

   The GUI opens and a dataset tab named "counter" is displayed in the Workspace (Figure 8-1).

**Figure 8-1. A Dataset in the Main Window Workspace**

![Dataset in the Main Window Workspace](image)

b. Right-click the `counter` instance and select **Add > To Wave > All items in region**.

   The waveforms display in the Wave window.

7. When you finish viewing the results, select **File > Quit** to close ModelSim.
Using Tcl with the Simulator

The DO files used in previous exercises contained only ModelSim commands. However, DO files are really just Tcl scripts. This means you can include a whole variety of Tcl constructs such as procedures, conditional operators, math and trig functions, regular expressions, and so forth.

In this exercise, you create a simple Tcl script that tests for certain values on a signal and then adds bookmarks that zoom the Wave window when that value exists. Bookmarks allow you to save a particular zoom range and scroll position in the Wave window.

1. Create the script.
   a. In a text editor, open a new file and enter the following lines:

   ```tcl
   proc add_wave_zoom {stime num} {
   echo "Bookmarking wave $num"
   bookmark add wave "bk$num" "[expr $stime - 50] [expr $stime + 100]" 0
   }
   ```

   These commands do the following:
   - Create a new procedure called "add_wave_zoom" that has two arguments, `stime` and `num`.
   - Create a bookmark with a zoom range from the current simulation time minus 50 time units to the current simulation time plus 100 time units.

   b. Now add these lines to the bottom of the script:

   ```tcl
   add wave -r /*
   when {clk'event and clk="1"} {
   echo "Count is [exa count]"
   if {[examine count] == "00100111"} {
   add_wave_zoom $now 1
   } elseif {[examine count] == "01000111"} {
   add_wave_zoom $now 2
   }
   }
   ```

   These commands do the following:
   - Add all signals to the Wave window.
   - Use a `when` statement to identify when `clk` transitions to 1.
   - Examine the value of `count` at those transitions and add a bookmark if it is a certain value.

   c. Save the script with the name "add_bkmrk.do."

   Save it into the directory you created in Basic Simulation.

2. Load the test_counter design unit.
a. Start ModelSim.

b. Select **File > Change Directory** and change to the directory you saved the DO file to in step 1c above.

c. Enter the following command at the QuestaSim> prompt:

```
vsim -voptargs="+acc" test_counter
```

3. Execute the DO file and run the design.

   a. Type **do add_bkmrk.do** at the VSIM> prompt.

   b. Type **run 1500 ns** at the VSIM> prompt.

      The simulation runs and the DO file creates two bookmarks.

   c. If the Wave window is docked in the Main window, click somewhere in the Wave window and select **Wave > Bookmarks > bk1**. If the window is undocked, select **View > Bookmarks > bk1** in the Wave window.

      Watch the Wave window zoom on and scroll to the time when `count` is 00100111. Try the `bk2` bookmark as well.

**Lesson Wrap-Up**

This concludes this lesson.

1. Select **File > Quit** to close ModelSim.
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9.4. THIS SECTION IS SUBJECT TO SECTION 6 ABOVE AND STATES THE ENTIRE LIABILITY OF MENTOR GRAPHICS AND ITS LICENSORS AND YOUR SOLE AND EXCLUSIVE REMEDY WITH RESPECT TO ANY ALLEGED PATENT OR COPYRIGHT INFRINGEMENT OR TRADE SECRET MISAPPROPRIATION BY ANY SOFTWARE LICENSED UNDER THIS AGREEMENT.

10. TERM. This Agreement remains effective until expiration or termination. This Agreement will immediately terminate upon notice if you exceed the scope of license granted or otherwise fail to comply with the provisions of Sections 1, 2, or 4. For any other material breach under this Agreement, Mentor Graphics may terminate this Agreement upon 30 days written notice if you are in material breach and fail to cure such breach within the 30 day notice period. If Software was provided for limited term use, this Agreement will automatically expire at the end of the authorized term. Upon any termination or expiration, you agree to cease all use of Software and return it to Mentor Graphics or certify deletion and destruction of Software, including all copies, to Mentor Graphics’ reasonable satisfaction.

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15. **CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION.** THIS AGREEMENT SHALL BE GOVERNED BY AND CONSTRUED UNDER THE LAWS OF THE STATE OF OREGON, USA, IF YOU ARE LOCATED IN NORTH OR SOUTH AMERICA, AND THE LAWS OF IRELAND IF YOU ARE LOCATED OUTSIDE OF NORTH OR SOUTH AMERICA. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply. Notwithstanding the foregoing, all disputes in Asia (except for Japan) arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the Chairman of the Singapore International Arbitration Centre (“SIAC”) to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section 15. This section shall not restrict Mentor Graphics’ right to bring an action against you in the jurisdiction where your place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.

16. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.

17. **PAYMENT TERMS AND MISCELLANEOUS.** You will pay amounts invoiced, in the currency specified on the applicable invoice, within 30 days from the date of such invoice. Any past due invoices will be subject to the imposition of interest charges in the amount of one and one-half percent per month or the applicable legal rate currently in effect, whichever is lower. Some Software may contain code distributed under a third party license agreement that may provide additional rights to you. Please see the applicable Software documentation for details. This Agreement may only be modified in writing by authorized representatives of the parties. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.

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