1. For an NMOS resistor with a resistive load as an inverter, show the steps and equations for the derivations of $V_{IL}$, $V_{OH}$, $V_{IH}$ and $V_{OL}$. (10 points)

2. Design a CMOS logic gate that implements the logic function $Y = A(BC + DE)$. (5 points)

3. For the TTL logic inverter interfaced with input and output, indicate with transistors are on and which are off, also indicate the voltages at points shown by $V$ and currents at points shown by $I$ in the figure below. Assume voltage drop of 0.7 volts across any PN junction that is forward biased. Also assume that when any transistor is saturated, the voltage across its collector and emitter is zero. (10 points)

4. For the following ECL circuit indicate the voltages at points shown by $V$ in the figure below and also the currents flowing in the two resistors. The two inputs (at left) are at -0.7 volts. (5 points)